JESD204B Survival Guide

Practical JESD204B Technical Information, Tips, and Advice from the World's Data Converter Market Share Leader*

*Analog Devices has a 48.5% global data converter market share, which is more than the next eight competitors combined, according to the analyst firm Databeans in its 2011 Data Converters Report.

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ANALOG DEVICES

Contents

What Is JESD204 and Why Should We Pay Attention to It?

by Jonathan Harris, Applications Engineer, Analog Devices, Inc.

A new converter interface is steadily picking up steam and looks to become the protocol of choice for future converters. This new interface, JESD204, was originally rolled out several years ago but has undergone revisions that are making it a much more attractive and efficient converter interface. As the resolution and speed of converters has increased, the demand for a more efficient interface has grown. The JESD204 interface brings this efficiency and offers several advantages over its CMOS and LVDS predecessors in terms of speed, size, and cost. Designs employing JESD204 enjoy the benefits of a faster interface to keep pace with the faster sampling rates of converters. In addition, there is a reduction in pin count which leads to smaller package sizes and a lower number of trace routes that make board designs much easier and offers lower overall system cost. The standard is also easily scalable so it can be adapted to meet future needs. This has already been exhibited by the two revisions that the standard has undergone. The JESD204 standard has seen two revisions since its introduction in 2006 and is now at Revision B. As the standard has been adopted by an increasing number of converter vendors and users, as well as FPGA manufacturers, it has been refined and new features have been added that have increased efficiency and ease of implementation. The standard applies to both analog-to-digital converters (ADCs), as well as digital-to-analog converters (DACs) and is primarily intended as a common interface to FPGAs (but may also be used with ASICs).

JESD204—WHAT IS IT?

In April of 2006, the original version of JESD204 was released. The standard describes a multigigabit serial data link between converter(s) and a receiver, commonly a device such as an FPGA or ASIC. In this original version of JESD204, the serial data link was defined for a single serial lane between a converter or multiple converters and a receiver. A graphical representation is provided in Figure 1. The lane shown is the physical interface between M number of converters and the receiver which consists of a differential pair of interconnect utilizing current mode logic (CML) drivers and receivers. The link shown is the serialized data link that is established between the converter(s) and the receiver. The frame clock is routed to both the converter(s) and the receiver and provides the clock for the JESD204 link between the devices.

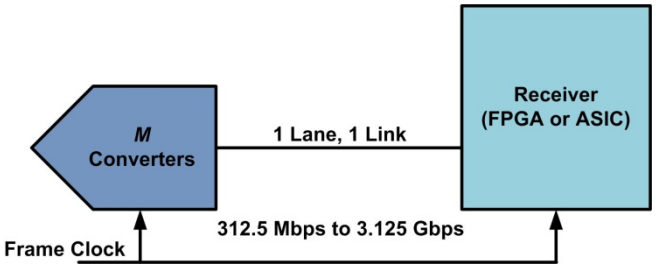

Figure 1. JESD204 Original Standard

The lane data rate is defined between 312.5 Megabits per second (Mbps) and 3.125 Gigabits per second (Gbps) with both source and load impedance defined as 100 Ω ±20%. The differential voltage level is defined as being nominally 800 mV peak-to-peak with a common-mode voltage level range from 0.72 V to 1.23 V. The link utilizes 8b/10b encoding which incorporates an embedded clock, removing the necessity for routing an additional clock line and the associated complexity of aligning an additional clock signal with the transmitted data a high data rates. It became obvious, as the JESD204 standard began gaining popularity, that the standard needed to be revised to incorporate support for multiple aligned serial lanes with multiple converters to accommodate increasing speeds and resolutions of converters.

This realization led to the first revision of the JESD204 standard in April of 2008 which became known as JESD204A. This revision of the standard added the ability to support multiple aligned serial lanes with multiple converters. The lane data rates, supporting from 312.5 Mbps up to 3.125 Gbps, remained unchanged as did the frame clock and the electrical interface specifications. Increasing the capabilities of the standard to support multiple aligned serial lanes made it possible for converters with high sample rates and high resolutions to meet the maximum supported data rate of 3.125 Gbps. Figure 2 shows a graphical representation of the additional capabilities added in the JESD204A revision to support multiple lanes.

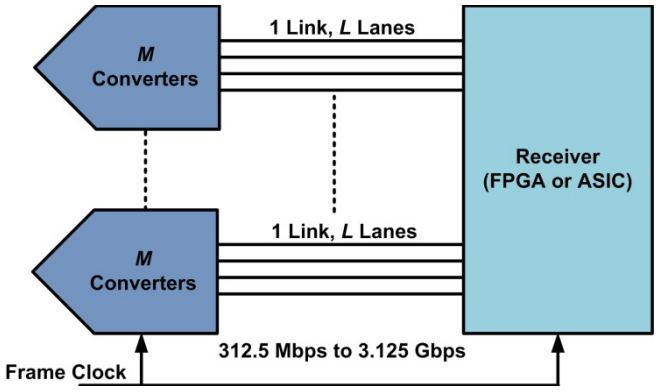

Figure 2. First Revision—JESD204A

Although both the original JESD204 standard and the revised JESD204A standard were higher performance than legacy interfaces, they were still lacking a key element. This missing element was deterministic latency in the serialized data on the link. When dealing with a converter, it is important to know the timing relationship between the sampled signal and its digital representation in order to properly recreate the sampled signal in the analog domain once the signal has been received (this situation is, of course, for an ADC, a similar situation is true for a DAC). This timing relationship is affected by the latency of the converter which is defined for an ADC as the number of clock cycles between the instant of the sampling edge of the input signal until the time that its digital representation is present at the converter's outputs. Similarly, in a DAC, the latency is defined as the number of clock cycles between the time the digital signal is clocked into the DAC until the analog output begins changing. In the JESD204 and JESD204A standards, there were no defined capabilities that would deterministically set the latency of the converter and its serialized digital inputs/outputs. In addition, converters were continuing to increase in both speed and resolution. These factors led to the introduction of the second revision of the standard, JESD204B.

In July of 2011, the second and current revision of the standard, JESD204B, was released. One of the key components of the revised standard was the addition of provisions to achieve deterministic latency. In addition, the data rates supported were pushed up to 12.5 Gbps, broken down into different speed grades of devices. This revision of the standard calls for the transition from using the frame clock as the main clock source to using the device clock as the main clock source. Figure 3 gives a representation of the additional capabilities added by the JESD204B revision.

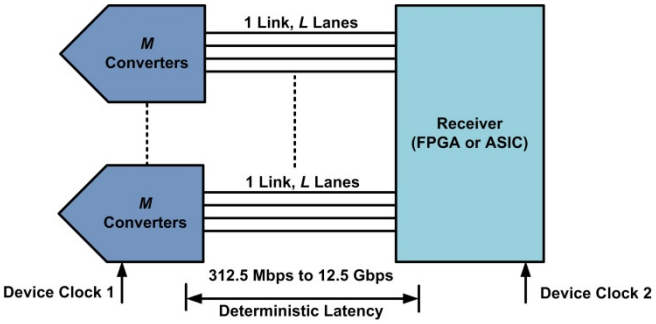

Figure 3. Second (Current) Revision—JESD204B

In the previous two versions of the JESD204 standard, there were no provisions defined to ensure deterministic latency through the interface. The JESD204B revision remedies this issue by providing a mechanism to ensure that, from power-up cycle to power-up cycle and across link re-synchronization events, the latency should be repeatable and deterministic. One way this is accomplished is by initiating the initial lane alignment sequence in the converter(s) simultaneously across all lanes at a well-defined moment in time by using an input signal called SYNC~. Another implementation is to use the SYSREF signal which is a newly defined signal for JESD204B. The SYSREF signal acts as the master timing reference and aligns all the internal dividers from device clocks as well as the local multiframe clocks in each transmitter and receiver. This helps to ensure deterministic latency through the system. The JESD204B specification calls out three device subclasses: Subclass 0—no support for deterministic latency, Subclass 1—deterministic latency using SYSREF, and Subclass 2—deterministic latency using SYNC~. Subclass 0 can simply be compared to a JESD204A link. Subclass 1 is primarily intended for converters operating at or above 500 MSPS while Subclass 2 is primarily for converters operating below 500 MSPS.

In addition to the deterministic latency, the JESD204B version increases the supported lane data rates to 12.5 Gbps and divides devices into three different speed grades. The source and load impedance is the same for all three speed grades being defined as 100 Ω ±20%. The first speed grade aligns with the lane data rates from the JESD204 and JESD204A versions of the standard and defines the electrical interface for lane data rates up to 3.125 Gbps. The second speed grade in JESD204B defines the electrical interface for lane data rates up to 6.375 Gbps. This speed grade lowers the minimum differential voltage level to 400 mV peak-to-peak, down from 500 mV peak-to-peak for the first speed grade. The third speed grade in JESD204B defines the electrical interface for lane data rates up to 12.5 Gbps. This speed grade lowers the minimum differential voltage level required for the electrical interface to 360 mV peak-to-peak. As the lane data rates increase for the speed grades, the minimum required

differential voltage level is reduced to make physical implementation easier by reducing required slew rates in the drivers.

To allow for more flexibility, the JESD204B revision transitions from the frame clock to the device clock. Previously, in the JESD204 and JESD204A revisions, the frame clock was the absolute timing reference in the JESD204 system. Typically, the frame clock and the sampling clock of the converter(s) were usually the same. This did not offer a lot of flexibility and could cause undesired complexity in system design when attempting to route this same signal to multiple devices and account for any skew between the different routing paths. In JESD204B, the device clock is the timing reference for each element in the JESD204 system. Each converter and receiver receives their respective device clock from a clock generator circuit which is responsible for generating all device clocks from a common source. This allows for more flexibility in the system design but requires that the relationship between the frame clock and device clock be specified for a given device.

JESD204—WHY SHOULD WE PAY ATTENTION TO IT?

In much the same way as LVDS began overtaking CMOS as the technology of choice for the converter digital interface several years ago, JESD204 is poised to tread a similar path in the next few years. While CMOS technology is still hanging around today, it has mostly been overtaken by LVDS. The speed and resolution of converters as well as the desire for lower power eventually renders CMOS and LVDS inadequate for converters. As the data rate increases on the CMOS outputs, the transient currents also increase and result in higher power consumption. While the current, and thus, power consumption, remains relatively flat for LVDS, the interface has an upper speed bound that it can support. This is due to the driver architecture, as well as the numerous data lines that must all be synchronized to a data clock. Figure 4 illustrates the different power consumption requirements of CMOS, LVDS, and CML outputs for a dual 14-bit ADC.

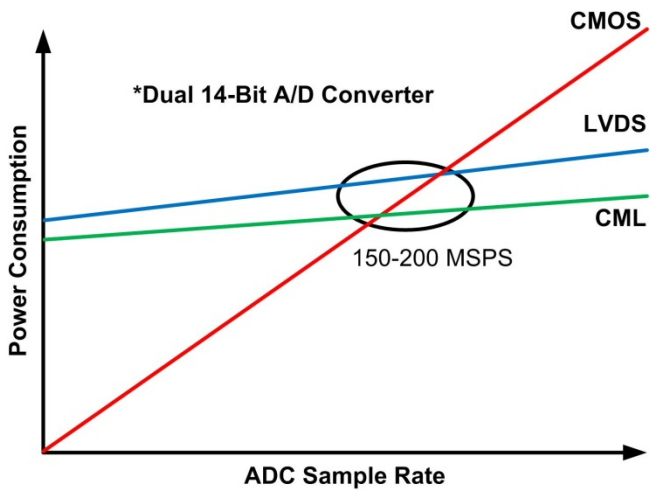

Figure 4. CMOS, LVDS, and CML Driver Power Comparison

At approximately 150 MSPS to 200 MSPS and 14 bits of resolution, CML output drivers start to become more efficient in terms of power consumption. CML offers the advantage of requiring less number of output pairs per a given resolution than LVDS and CMOS drivers due to the serialization of the data. The CML drivers specified for the JESD204B interface have an additional advantage since the specification calls for reduced peak-to-peak voltage levels as the sample rate increases and pushes up the output line rate. The number of pins required for the same give converter resolution and sample rate is also considerably less. Table 1 gives an illustration of the pin counts for the three different interfaces using a 200 MSPS converter with various channel counts and bit resolutions. The data assumes a synchronization clock for each channel's data in the case of the CMOS and LVDS outputs and a maximum data rate of 4.0 Gbps for JESD204B data transfer using the CML outputs. The reasons for the progression to JESD204B using CML drivers become obvious when looking at this table and observing the dramatic reduction in pin count that can be achieved.

Table 1. Pin Count Comparison—200 MSPS ADC

Number of Channels	Resolution	CMOS Pin Count	LVDS Pin Count (DDR)	CML Pin Count (JESD204B)
1	12	13	14	2
2	12	26	28	4
4	12	52	56	8
8	12	104	112	16
1	14	15	16	2
2	14	30	32	4
4	14	60	64	8
8	14	120	128	16
1	16	17	18	2
2	16	34	36	4
4	16	68	72	8
8	16	136	144	16

Analog Devices, Inc., market leader in data converters, has seen the trend that is pushing the converter digital interface towards the JESD204 interface defined by JEDEC. Analog Devices has been involved with the standard from the beginning when the first JESD204 specification was released. To date, Analog Devices has released to production several converters with the JESD204 and JESD204A compatible outputs and is currently developing products with outputs that are compatible with JESD204B. The AD9639 is a quad-channel 12-bit 170 MSPS/210 MSPS ADC that has a JESD204 interface. The AD9644 and AD9641 are 14-bit 80 MSPS/155 MSPS dual and single ADCs that have the JESD204A interface. From the DAC perspective, the recently released AD9128 is a dual 16-bit 1.25 GSPS DAC that has a JESD204A interface. For more information on Analog Devices efforts in regards to JESD204, please visit www.analog.com/jesd204.

As the speed and resolution of converters have increased, the demand for a more efficient digital interface has increased. The industry began realizing this with the JESD204 serialized data interface. The interface specification has continued to evolve to offer a better and faster way to transmit data between converters and FPGAs (or ASICs). The interface has undergone two revisions to improve upon its implementation and meet the increasing demands brought on by higher speeds and higher resolution converters. Looking to the future of converter digital interfaces, it is clear that JESD204 is poised to become the industry choice for the digital interface to converters. Each revision has answered the demands for improvements on its implementation and has allowed the standard to evolve to meet new requirements brought on by changes in converter technology. As system designs become more complex and converter performance pushes higher, the JESD204 standard should be able to adapt and evolve to continue to meet the new design requirements necessary.

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High Speed Converter Survival Guide: Digital Data Outputs

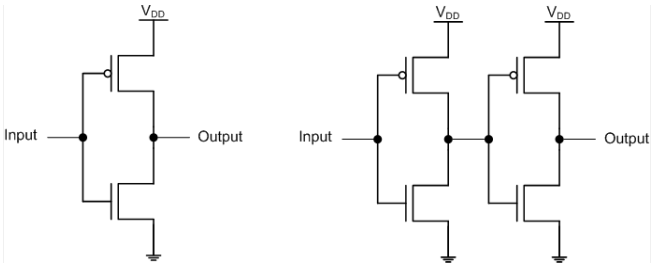
by Jonathan Harris, Product Applications Engineer, Analog Devices, Inc.

IDEA IN BRIEF

With a multitude of analog-to-digital converters (ADCs) available for designers to choose from, an important parameter to consider in the selection process is the type of digital data outputs included. Currently, the three most common types of digital outputs utilized by high speed converters are complementary metal oxide semiconductor (CMOS), low voltage differential signaling (LVDS), and current mode logic (CML). Each of these digital output types used in ADCs has its advantages and disadvantages that designers should consider in their particular application. These factors depend on the sampling rate and resolution of the ADC, the output data rates, the power requirements of the system design, and others. In this article, the electrical specifications of each type of output will be discussed along with what makes each type suited for its particular application. These different types of outputs will be compared in terms of physical implementation, efficiency, and the applications best suited for each type.

CMOS DIGITAL OUTPUT DRIVERS

In ADCs with sample rates of less than 200 MSPS, it is common to find that the digital outputs are CMOS. A typical CMOS driver employed consists of two transistors, one NMOS and one PMOS, connected between the power supply (V_{DD}) and ground, as shown in Figure 1a. This structure results in an inversion in the output, so as an alternative, the back-to-back structure in Figure 1b can be used in order to avoid the inversion in the output. The input of the CMOS output driver is high impedance while the output is low impedance. At the input to the driver, the impedance of the gates of the two CMOS transistors is quite high since the gate is isolated from any conducting material by the gate oxide. The impedances at the input can range from kilo ohms to mega ohms. At the output of the driver, the impedance is governed by the drain current, I_D, which is typically small. In this case, the impedance is usually less than a few hundred ohms. The voltage levels for CMOS swing from approximately V_{DD} to ground and can, therefore, be quite large depending on the magnitude of V_{DD}.



a) Inverted Output b) Noninverted Output

Figure 1. Typical CMOS Digital Output Driver

Since the input impedance is high and the output impedance is relatively low, an advantage that CMOS has is that one output can typically drive multiple CMOS inputs. Another advantage to CMOS is the low static current. The only instance where there is significant current flow is during a switching event on the CMOS driver. When the driver is in either a low state, pulled to ground, or in a high state, pulled to V_{DD}, there is little current flow through the driver. However, when the driver is switching from a low state to a high state or from a high state to a low state, there is a momentary low resistance path from V_{DD} to ground. This transient current is one of the main reasons why other technologies are used for output drivers when converter speeds go beyond 200 MSPS.

Another reason to note is that a CMOS driver is required for each bit of the converter. If a converter has 14 bits, there are 14 CMOS output drivers required to transmit each of those bits. Commonly, more than one converter is placed in a given package, and up to eight converters in a single package are common. When using CMOS technology, this could mean that there would be up to 112 output pins required just for the data outputs. Not only would this be inhibitive from a packaging standpoint, but it would also have high power consumption and increase the complexity of board layout. To combat these issues, an interface using low voltage differential signaling (LVDS) was introduced.

LVDS DIGITAL OUTPUT DRIVERS

LVDS offers some nice advantages over CMOS technology. It operates with a low voltage signal, approximately 350 mV, and is differential rather than single ended. The lower voltage swing has a faster switching time and reduces EMI concerns. By virtue of being differential, there is also the benefit of

common-mode rejection. This means that noise coupled to the signals tends to be common to both signal paths and is mostly cancelled out by the differential receiver. The impedances in LVDS need to be more tightly controlled. In LVDS, the load resistance needs to be approximately 100 Ω and is usually achieved by a parallel termination resistor at the LVDS receiver. In addition, the LVDS signals need to be routed using controlled impedance transmission lines. The single-ended impedance required is 50 Ω while the differential impedance is maintained at 100 Ω. Figure 2 shows the typical LVDS output driver.

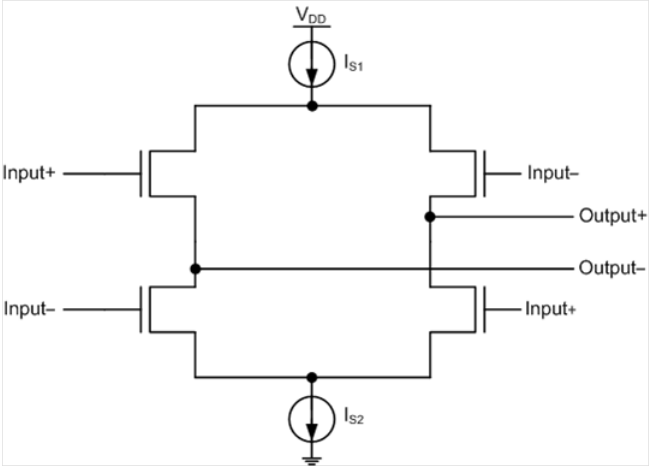


Figure 2. Typical LVDS Output Driver

As can be seen by the topology of the LVDS output driver in Figure 2, the circuit operation results in a fixed dc load current on the output supplies. This avoids current spikes that would be seen in a typical CMOS output driver when the output logic state transitions. The nominal current source/sink in the circuit is set to 3.5 mA which results in a typical output voltage swing of 350 mV with a 100 Ω termination resistor. The common-mode level of the circuit is typically set to 1.2 V, which is compatible with 3.3 V, 2.5 V, and 1.8 V supply voltages.

There are two standards that have been written to define the LVDS interface. The most commonly used is the ANSI/TIA/EIA-644 specification entitled "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits." The other is the IEEE standard 1596.3 entitled "IEEE Standard for Low Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)."

LVDS does require that special attention be paid to the physical layout of the routing of the signals but offers many advantages for converters when sampling at speeds of 200 MSPS or greater. The constant current of the LVDS driver allows for many outputs to be driven without the large amount of current draw that CMOS would require. In addition, it is possible to operate LVDS in a double-data rate (DDR) mode where two data bits can be routed through the same LVDS output driver. This reduces the number of pins required by one half compared to CMOS. In addition, the amount of power consumed for the same number of data outputs is reduced. LVDS does offer numerous benefits over CMOS for the data outputs of converters, but it eventually has its limitations as CMOS does. As converter resolution increases, the number of data outputs required by an LVDS interface becomes more difficult to manage for PCB layouts. In addition, the sample rates of converters eventually push the required data rates of the interface beyond the capabilities of LVDS.

CML OUTPUT DRIVERS

The latest trend in digital output interfaces for converters is to use a serialized interface that uses current mode logic (CML) output drivers. Typically, converters with higher resolutions (≥14 bits), higher speeds (≥200 MSPS), and the desire for smaller packages with less power utilize these types of drivers. The CML output driver is employed in JESD204 interfaces that are being used on the latest converters.

Utilizing CML drivers with serialized JESD204 interfaces allows data rates on the converter outputs to go up to 12 Gbps (with the current revision of the specification JESD204B). In addition, the number of output pins required is dramatically reduced. Routing a separate clock signal is no longer necessary since the clock becomes embedded in the 8b/10b encoded data stream. The number of data output pins is also reduced with a minimum of two being required. As the resolution, speed, and channel count of the converter increase, the number of data output pins may be scaled to account for the greater amount of throughput required. Since the interface employed with CML drivers is typically serial, however, the increase in the number of pins required is much smaller than that compared with CMOS or LVDS (the data transmitted in CMOS or LVDS is parallel, which requires a much great number of pins).

Since CML drivers are employed in serialized data interfaces, the number of pins required is much smaller. Figure 3 shows a typical CML driver used for converters with JESD204 or similar data outputs. The figure gives a generalization of the typical architecture of a CML driver. It shows the optional source termination resistor and the common-mode voltage. The inputs to the circuit drive the switches to the current sources which drive the appropriate logic value to the two output terminals.

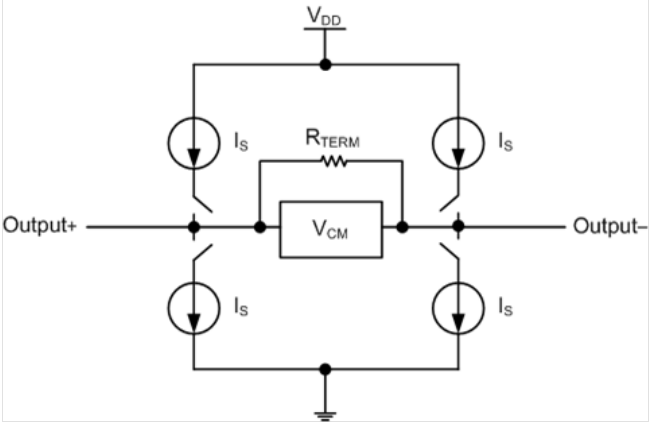


Figure 3. Typical CML Output Driver

A CML driver is similar to the LVDS driver in that it operates in a constant current mode. This also gives the CML driver an advantage in terms of power consumption. Operating in a constant current mode requires fewer output pins, and the total power consumption is reduced. As with LVDS, a load termination is required, as well as controlled impedance transmission lines having a single-ended impedance of 50 Ω and a differential impedance of 100 Ω. The driver itself may also have terminations, as shown in Figure 3, to help with any signal reflections due to the sensitivity with such high bandwidth signals. In converters employing the JESD204 standard, there are different specifications for the differential and common-mode voltage levels depending upon the speed of operation. Operating at speeds up to 6.375 Gbps, the differential voltage level is nominally 800 mV while the common mode is approximately 1.0 V. When operating above speeds of 6.375 Gbps, but less than 12.5 Gbps, the differential voltage level is specified at 400 mV while the common mode is again approximately 1.0 V. As converter speed and resolution increase, CML outputs look to be the desired driver type to deliver the speeds necessary to keep pace with technology demands placed on converters for their various applications.

DIGITAL TIMING—THINGS TO LOOK OUT FOR

Each of the digital output driver types has timing relationships that need to be monitored closely. Since there are multiple data outputs with CMOS and LVDS, attention must be directed to the routing paths of the signals to minimize skew. If there is too large of a difference, then proper timing at the receiver may not be achieved. In addition, there is a clock signal that needs to be routed and aligned with the data outputs. Careful attention must be given to the routing paths between the clock output, and also the data outputs, to ensure that the skew is not too large.

In the case of CML in the JESD204 interface, attention must also be directed to the routing paths between the digital outputs. There are significantly less data outputs to manage, so this task does become easier but cannot be neglected altogether. In this case, there should be no concern with regards to timing skew between the data outputs and the clock output since the clock is embedded in the data. However, attention must be given to an adequate clock and data recovery (CDR) circuit in the receiver.

In addition to the skew, the setup and hold times must also be given attention with CMOS and LVDS. The data outputs must be driven to their appropriate logic state in sufficient time before the edge transition of the clock and must be maintained in that logic state for a sufficient time after the edge transition of the clock. This can be affected by the skew between the data outputs and the clock outputs, so it is important to maintain good timing relationships. LVDS has the advantage over CMOS due to the lower signal swings and differential signaling. The LVDS output driver does not have to drive such a large signal to many different outputs and does not draw a large amount of current from the power supply when switching logic states, as the CMOS driver would. This makes it less likely for there to be an issue delivering a change in logic state. If there were many CMOS drivers switching simultaneously, the power supply voltage could get pulled down and introduce issues driving the right logic values to the receiver. The LVDS drivers would maintain a constant level of current such that this particular issue would not arise. In addition, the LVDS drivers are inherently more immune to common-mode noise due to its use of differential signaling. The CML drivers have similar benefits to LVDS. These drivers also have a constant level of current, but unlike LVDS, fewer numbers are required due to the serialization of the data. In addition, the CML drivers also offer immunity to common-mode noise since they also use differential signaling.

As converter technology has progressed with increased speeds and resolutions, the digital output drivers have adapted and evolved to meet the requirements necessary to transmit data. CML outputs are becoming more popular as the digital output interfaces in converters transition to serialized data transmission. However, CMOS and LVDS digital outputs are still being utilized today in current designs. There are applications where each type of digital output is best suited and makes the most sense to use. Each type of output comes with challenges and design considerations, and each type of output has its advantages. In converters with sampling speeds less than 200 MSPS, CMOS is still an appropriate technology to employ. When sampling speeds increase above 200 MSPS, LVDS becomes a more viable option in many applications as compared to CMOS. To further increase

efficiency and reduce power and package size, CML drivers can be employed with a serialized data interface such as JESD204.

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JESD204B vs. Serial LVDS Interface Considerations for Wideband Data Converter Applications

by George Diniz, Product Line Manager, Analog Devices, Inc.

IDEA IN BRIEF

The JESD204A/JESD204B industry standard for serial interfaces was developed to address the problem of interconnecting the newest wideband data converters with other system ICs in an efficient and cost saving manner. The motivation was to standardize an interface that would reduce the number of digital inputs/outputs between data converters and other devices, such as FPGAs (field programmable gate arrays) and SoCs (systems on a chip), through the use of a scalable high speed serial interface.

Trends show that new applications, as well as advances in existing ones, are driving the need for wideband data converters with increasingly higher sampling frequencies and data resolutions. Transmitting data to and from these wideband converters poses a significant design problem as bandwidth limitations of existing I/O technologies force the need for higher pin counts on converter products. Consequently, systems PCB designs have become increasingly more complex in terms of interconnect density. The challenge is routing a large number of high speed digital signals while managing electrical noise. The ability to offer wideband data converters with GSPS sampling frequencies, using fewer interconnects, simplifies the PCB layout challenges and allows for smaller form factor realization without impacting overall system performance.

Market forces continue to press for more features, functionality, and performance in a given system, driving the need for higher data-handling capacity. The high speed analog-to-digital converter and digital-to-analog converter-to-FPGA interface had become a limiting factor in the ability of some system OEMs to meet their next generation data-intensive demands. The JESD204B serial interface specification was specifically created to help solve this problem by addressing this critical data link. Figure 1 shows typical high speed converter-to-FPGA interconnect configurations using JESD204A/JESD204B.

Some key end-system applications that are driving the deployment of this specification, as well as a contrast between serial LVDS and JESD204B, are the subject of the remainder of the article.

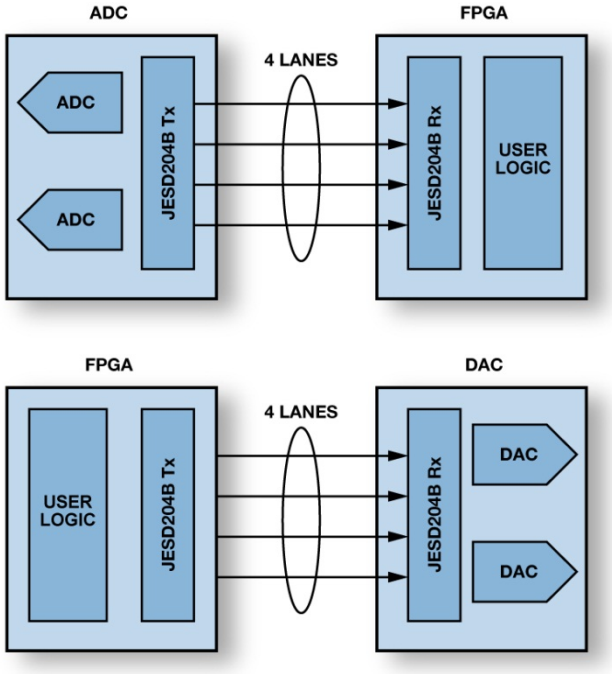

Figure 1. Typical High Speed Converter to FPGA Interconnect Configurations Using JESD204A/JESD204B Interfacing (Source: Xilinx)

THE APPLICATIONS DRIVING THE NEED FOR JESD204B

Wireless Infrastructure Transceivers

OFDM based technologies, such as LTE, used in today's wireless infrastructure transceivers use DSP blocks implemented on FPGAs or SoC devices driving antenna array elements to generate beams for each individual subscriber's handset. Each array element can require movement of hundreds of megabytes of data per second between FPGAs and data converters in both transmit or receive modes.

Software Defined Radios

Today's software defined radios utilize advanced modulation schemes that can be reconfigured on the fly, and rapidly increasing channel bandwidths, to deliver unprecedented wireless data rates. Efficient, low power, low pin count FPGA-to-data converter interfaces in the antenna path play a critical role in their performance. Software defined radio architectures are integral to the transceiver infrastructure

for multicarrier, multimode wireless networks supporting GSM, EDGE, W-CDMA, LTE, CDMA2000, WiMAX, and TD-SCDMA.

Medical Imaging Systems

Medical imaging systems including ultrasound, computational tomography (CT) scanners, magnetic resonance imaging (MRI), and others generate many channels of data that flow through a data converter to FPGAs or DSPs. Continually increasing I/O counts are driving up the number of components by requiring the use of interposers to match FPGA and converter pin out and increasing PCB complexity. This adds additional cost and complexity to the customer's system that can be solved by the more efficient JESD204B interface.

Radar and Secure Communications

Increasingly sophisticated pulse structures on today's advanced radar receivers are pushing signal bandwidths toward 1 GHz and higher. Latest generation active electronically scaled array (AESA) radar systems may have thousands of elements. High bandwidth SERDES-based serial interfaces are needed to connect the array element data converters to the FPGAs or DSPs that process incoming and generate outgoing data streams.

SERIAL LVDS VS. JESD204B

Choosing Between Series LVDS and JESD204B Interface

In order to best select between converter products that use either LVDS or the various versions of the JESD204 serial interface specification, a comparison of the features and capabilities of each interface is useful. A short tabular comparison is provided in Table 1. At the SerDes level, a notable difference between LVDS and JESD204 is the lane data rate, with JESD204 supporting greater than three times the serial link speed per lane when compared with LVDS. When comparing the high level features like multidevice synchronization, deterministic latency, and harmonic clocking, JESD204B is the only interface that provides this functionality. Systems requiring wide bandwidth multichannel converters that are sensitive to deterministic latency across all lanes and channels won't be able to effectively use LVDS or parallel CMOS.

Table 1. Comparison Between Serial LVDS and JESD204 Specifications

Function	Serial LVDS	JESD204	JESD204A	JESD204B
Specification Release	2001	2006	2008	2011
Maximum lane Rate	1.0 Gbps	3.125 Gbps	3.125 Gbps	12.5 Gbps
Multiple Lanes	No	No	Yes	Yes
Lane Synchronization	No	No	Yes	Yes
Multidevice Synchronization	No	Yes	Yes	Yes
Deterministic Latency	No	No	No	Yes
Harmonic Clocking	No	No	No	Yes

LVDS OVERVIEW

Low voltage differential signaling (LVDS) is the traditional method of interfacing data converters with FPGAs or DSPs. LVDS was introduced in 1994 with the goal of providing higher bandwidth and lower power dissipation than the existing RS-422 and RS-485 differential transmission standards. LVDS was standardized with the publication of TIA/EIA-644 in 1995. The use of LVDS increased in the late 1990s and the standard was revised with the publication of TIA/EIA-644-A in 2001.

LVDS uses differential signals with low voltage swings for high speed data transmission. The transmitter typically drives ±3.5 mA with a polarity matching the logic level to be sent through a 100 Ω resistor, generating a ±350 mV voltage swing at the receiver. The always-on current is routed in different directions to generate logic ones and zeros. The always-on nature of LVDS helps eliminate simultaneous switching noise spikes and potential electromagnetic interference that sometimes occur when transistors are turned on and off in single-ended technologies. The differential nature of LVDS also provides considerable immunity to common-mode noise sources. The TIA/EIA-644-A standard recommends a maximum data rate of 655 Mbps, although it predicts a possible speed of over 1.9 Gbps for an ideal transmission medium.

The huge increase in the number and speed of data channels between FPGAs or DSPs and data converters, particularly in the applications described earlier, has created several issues with the LVDS interface (see Figure 2). The bandwidth of a differential LVDS wire is limited to about 1.0 Gbps in the real world. In many current applications, this creates the need for a substantial number of high bandwidth PCB interconnects, each of which is a potential failure point. The large number of traces also increases PCB complexity or overall form

factor, which raises both design and manufacturing costs. In some applications, the data converter interface becomes the limiting factor in achieving the required system performance in bandwidth hungry applications.

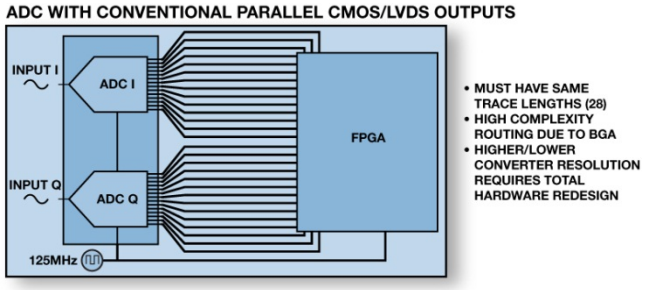

Figure 2. Challenges in System Design and Interconnect Using Parallel CMOS or LVDS

JESD204B OVERVIEW

The JESD204 data converter serial interface standard was created by the JEDEC Solid State Technology Association JC-16 Committee on Interface Technology with the goal of providing a higher speed serial interface for data converters to increase bandwidth and reduce the number of digital inputs and outputs between high speed data converters and other devices. The standard builds on 8b/10b encoding technology developed by IBM that eliminates the need for a frame clock and a data clock, enabling single line pair communications at a much higher speed.

In 2006, JEDEC published the JESD204 specification for a single 3.125 Gbps data lane. The JESD204 interface is self-synchronous, so there is no need to calibrate the length of the PCB wire traces to avoid clock skew. JESD204 leverages the SerDes ports offered on many FPGAs to free up general-purpose I/O.

JESD204A, published in 2008, adds support for multiple time-aligned data lanes and lane synchronization. This enhancement makes it possible to use higher bandwidth data converters and multiple synchronized data converter channels and is particularly important for wireless infrastructure transceivers used in cellular base stations. JESD204A also provides multidevice synchronization support which is useful for devices, such as medical imaging systems, that use large numbers of ADCs.

JESD204B, the third revision of the spec, increases the maximum lane rate to 12.5 Gbps. JESD204B also adds deterministic latency, which communicates synchronization status between the receiver and transmitter. Harmonic clocking, also introduced in JESD204B, makes it possible to derive a high speed data converter clock from a lower speed input clock with deterministic phasing.

SUMMARY

The JESD204B industry serial interface standard reduces the number of digital inputs and outputs between high speed data converters and FPGAs and other devices. Fewer interconnects simplify layout and make it possible to achieve a smaller form factor (see Figure 3). These advantages are important for a wide range of high speed data converter applications, such as wireless infrastructure transceivers, software defined radios, medical imaging systems, and radar and secure communications. Analog Devices, Inc., is an original participating member of the JESD204 standards committee and we have concurrently developed compliant data converter technology and tools along with a comprehensive product roadmap offering. By providing customers with products that combine our cutting edge data converter technology along with the JESD204A/JESD204B interface, we expect to enable customers to solve their system design problems, while taking advantage of this significant interfacing breakthrough.

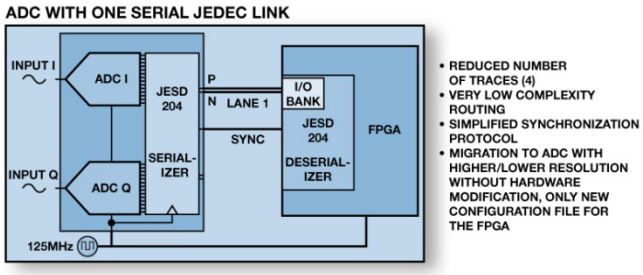

Figure 3. JESD204 with Its High Speed Serial I/O Capability Solves the System PCB Complexity Challenge

ABOUT THE AUTHOR

George Diniz is a Product Line Manager in the High Speed Digital-to-Analog Converters Group at Analog Devices in Greensboro, NC. He leads a team responsible for the development of JESD204B Rx and Tx interface cores, which are integrated into high speed analog-to-digital and digital-to-analog converter products. He has 25 years of experience in the semiconductor industry and has held various roles in design engineering and product line management. Before joining ADI, George was a design engineer at IBM, where he was engaged in mixed-signal design of custom SRAM macros, PLL, and DLL functions for PowerPC processors. He has an MSEE from North Carolina State University and a BEE from Manhattan College. For recreation, George enjoys outdoor activities, restoring automobiles, and running.

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ANALOG DEVICES

Grasp the Critical Issues for a Functioning JESD204B Interface

by Anthony Desimone, Applications Engineer, Analog Devices, Inc., and Michael Giancioppo, Applications Engineer, Analog Devices.

JESD204B is a recently approved JEDEC Standard for serial data interfacing between converters and digital processing devices. As a third-generation standard, it addresses some of the limitations of the earlier versions. Among the benefits of this interface are reductions in required board area for data interface routing, reductions in setup and hold timing requirements, and the enablement of smaller packages for converter and logic devices. New analog/digital converters from various vendors, such as the AD9250 from Analog Devices, Inc., use this interface.

There is a trade-off to realizing the benefits of the JESD204B interface, as it has complexities and subtleties which distinguish it from existing interface formats and protocols. As with any standard, it is clear that the interface must function seamlessly to gain popularity and traction versus more common interfaces, such as single data rate or double data rate CMOS or LVDS. Although the JESD204B standard is documented by JEDEC, some specific information about it is subject to interpretation or may be spread over multiple references. It is also obvious that it would be extremely helpful if there were a concise guide that provided an overview of the standard, how it works, and how to troubleshoot it if issues arise.

This article explains the interface from an ADC to FPGA for JESD204B, how to identify when it's working correctly, and, perhaps more important, how to troubleshoot it if something isn't quite right. The troubleshooting techniques discussed can use commonly available test and measurement equipment including oscilloscopes and logic analyzers, along with software tools such as the ChipScope from Xilinx® or SignalTap from Altera®. Interface signaling is also explained to allow a single approach or multiple approaches to visualize the signaling.

JESD204B OVERVIEW

The JESD204B standard provides a method to interface one or multiple data converters to a digital-signal processing device (typically, an ADC or DAC to an FPGA) over a higher speed serial interface compared to the more typical parallel data transfers. The interface, which runs at up to 12.5 Gbps/lane, uses a framed serial data link with embedded clock and alignment characters. The interface eases implementation of the data interface of high speed converters by reducing the number of traces between devices, thus reducing trace-matching requirements, and removing setup- and hold-timing constraint issues. Since a link needs to be established prior to data transfer, there are new challenges and techniques required to identify that the interface is working properly and, if not, what to do.

Starting with a brief explanation of how the standard works, the JESD204B interface uses three phases to establish the synchronized link: code group synchronization (CGS), initial lane synchronization (ILAS), and data transmission phase. Required signals for the link are a shared reference clock (device clock), at least one differential CML physical data electrical connection (called a lane), and at least one other synchronization signal (SYNC~ and possibly SYSREF). The signals used depend upon the subclass:

- Subclass 0 uses device clock, lanes, and SYNC~
- Subclass 1 uses device clock, lanes, SYNC~, and SYSREF
- Subclass 2 uses device clock, lanes, and SYNC~

Subclass 0 is adequate in many cases and will be the focus of this article. Subclass 1 and Subclass 2 provide a method to establish deterministic latency. This is important in application when synchronizing multiple devices or system synchronization or fixed latency is required (such as when a system needs a known sampling edge for an event or an event must react to an input signal within a specified time).

Figure 1 shows a simplified JESD204B link from the Tx device (ADC) to the Rx device (FPGA), with data from one ADC going over one lane.

Although there are many variables within the JESD204B specification, some have particular importance when establishing a link. These key variables from the specification are (note that these values are typically represented as "X – 1"):

- M: number of converters.
- L: number of physical lanes.
- F: number of octets per frame.
- K: number of frames per multiframe.
- N and N': converter resolution and number of bits used per sample (multiple of 4), respectively. N' value is N value, plus control and dummy bits.

SUBCLASS 0: SYNCHRONIZATION STEPS

As noted above, many applications can use the relatively simpler Subclass 0 mode of operation. This is also the easiest mode to establish and for which to verify a link. Subclass 0 uses three phases to establish and monitor synchronization: CGS phase, ILAS phase, and data phase. The figures associated with each phase present the data in different formats, as they might be seen on an oscilloscope, logic analyzer, or FPGA virtual I/O analyzer such as Xilinx ChipScope or Altera SignalTap.

The Code Group Synchronization (CGS) Phase

The most significant parts of the CGS phase that can be observed over the link are shown in Figure 2, along with a description of the five highlighted points of the figure.

1. The Rx issues a synchronization request by driving the SYNC~ pin low.
2. The Tx transmits /K28.5/ symbols (10 bits/symbol), unscrambled beginning on the next symbol.
3. The Rx synchronizes when it receives at least four consecutive /K28.5/ symbols without error and then the Rx drives the SYNC~ pin high.
4. Rx must receive at least four 8B/10B characters without error otherwise synchronization fails and the link stays in CGS phase.
5. CGS Phase ends and ILAS phase begins.

The /K28.5/ character, also just known as /K/, within the JESD204B standard can be exhibited as shown in Figure 3. The standard requires a running neutral disparity. The 8B10B coding allows a balanced sequence that, on average, contains an equal amount of 1's and 0's. Each 8B10B character can have a positive (more 1's) or negative (more 0's) disparity, and the parity of the current character is determined by the current sum of the previous characters sent, and this is typically accomplished by alternately transmitting a positive parity word, followed by a negative parity word; the figure shows both polarities of the /K28.5/ symbol.

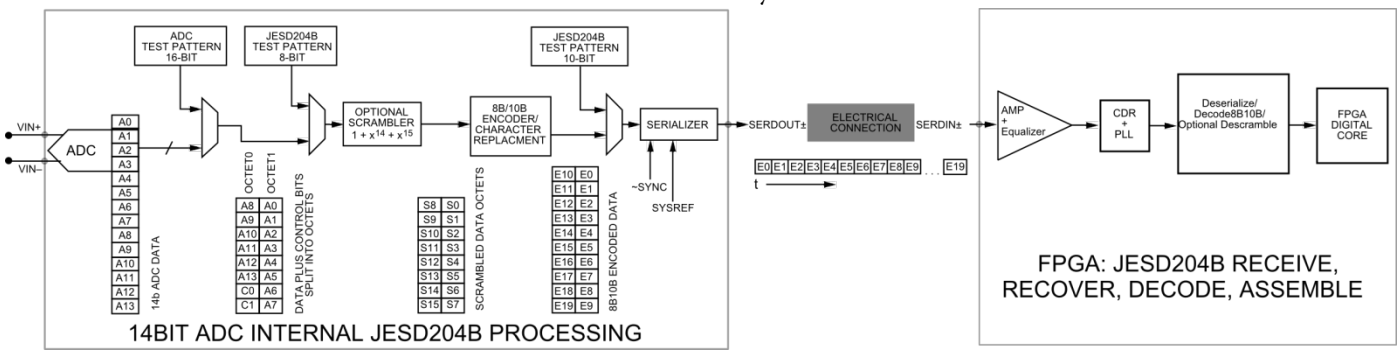

Figure 1. JESD204B Link Diagram for One ADC to an FPGA through One Lane

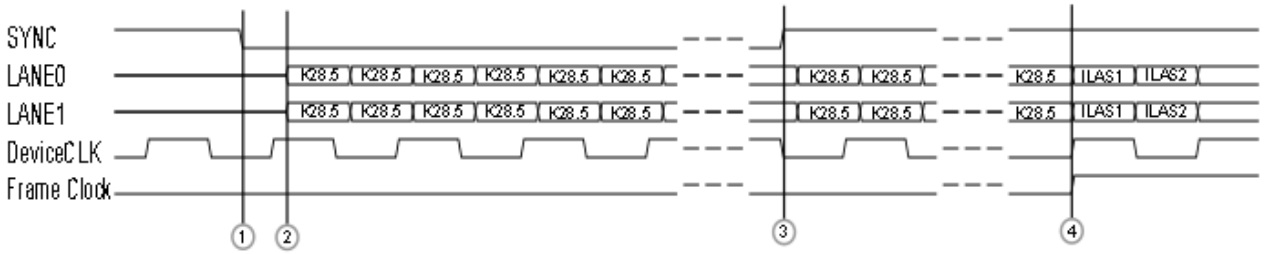

Figure 2. Logic Output of JESD204B Subclass 0 Link Signals During CGS Phase (Assumes Two Lanes, One Device with Two ADCs)

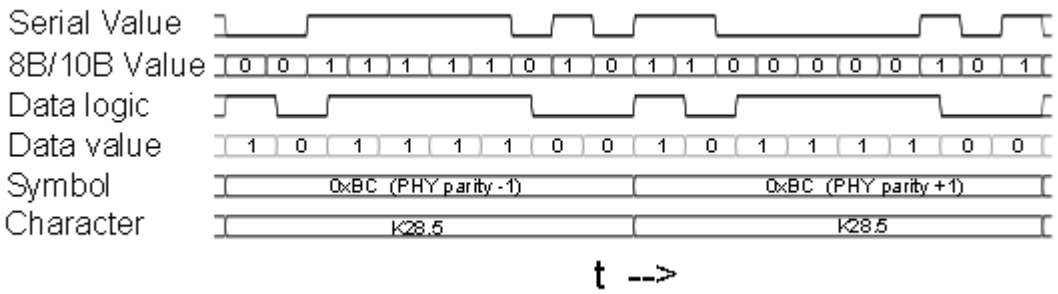

Figure 3. Logic Output of /K28.5/ Characters and How It Propagates through the JESD204B Tx Signal Path

Note these key points:

- *Serial Value* represents the logic levels of the 10 bits transmitted over the lane, as would be seen by an oscilloscope measuring the physical interface.
- *8B/10B Value* represents the logic values (10 bits) transmitted over the lane, as might be seen by a logic analyzer measuring the physical interface.
- *Data value* and *Data logic* represent the logic levels of the symbol inside the JESD204B Tx block before 8B10B coding, as would be seen on an FPGA logic analysis tool such as Xilinx ChipScope or Altera SignalTap.
- *Symbol* represents the hex value of the character that is to be transmitted, noting parity for PHY layer
- *Character* is shown to indicate the JESD204B character as it is referred to in the JEDEC specification.

THE ILAS PHASE

In the ILAS phase, there are four multiframes which allow the Rx to align lanes from all links and also allows the Rx to verify the link parameters. Alignment is required to accommodate trace length differences and any character skew the receivers introduce. Each successive multiframe immediately follows the previous one of four (Figure 4). Whether or not the scrambling link parameter is enabled, ILAS is always transmitted without scrambling.

The ILAS phase begins after SYNC~ has been deasserted (goes high). After the transmit block has internally tracked (within the ADC) a full multiframe, it will begin to transmit four multiframes. Dummy samples are inserted between the required characters so that full multiframes are transmitted (Figure 4). The four multiframes consist of the following:

- Multiframe 1: begins with an /R/ character [K28.0] and ends with an /A/ character [K28.3].
- Multiframe 2: begins with an /R/ character followed by a /Q/ [K28.4] character, followed by link configuration parameters over 14 configuration octets (Table 1), and ends with an /A/ character.
- Multiframe 3: the same as Multiframe 1.
- Multiframe 4: the same as Multiframe 1.

The frame length can be calculated for the JESD204B parameters: (S) × (1/Sample Rate).

> Translation: (Number of Samples / Converter / Frame) × (1/Sample Rate)
>
> Example: a converter that has one sample per converter per frame (Note "S" is 0 in this case since it is encoded as Binary value –1) and the converter is running at 250 MSPS has a 4 ns frame length
>
> (1) × (1/250 MHz) = 4 ns

The multiframe length can be calculated for the JESD204B parameters: K × S × (1/Sample Rate)

> Translation: (Number of Samples / Converter / Frame) × (Number of Frames / Multiframe) × (1/Sample Rate)
>
> Example: a converter that has one sample per converter per frame, 32 frames per multiframes, and the converter running at 250 MSPS has a 128 ns multiframe length
>
> (1) × (32) × (1/250 MHz) = 128 ns

DATA PHASE WITH CHARACTER REPLACEMENT ENABLED

In the data transmission phase, frame alignment is monitored with control characters. Character replacement is used at the end of frames. There is no additional overhead to accommodate data or frame alignment during the data phase. Character replacement allows an alignment character to be issued at a frame boundary "if and only if" the last character of the current frame may be replaced with the last character of the last frame, facilitating (occasional) confirmation that the alignment has not changed since the ILAS sequence.

Character replacement in the transmitter occurs in the following instances:

- If scrambling is disabled and the last octet of the frame or multiframe equals the octet value of the previous frame.
- If scrambling is enabled and the last octet of the multiframe is equal to 0x7C, or the last octet of a frame is equal to 0xFC.

Transmitters and receivers each maintain a multiframe counter (LMFC) that perpetually count to (F × K) − 1 and then wrap back to "0" to count again (ignoring internal word width). A common (sourced) SYSREF is issued to all transmitters and receivers which use the SYSREF to reset their LMFCs, after which all LMFCs should be synchronized (within one clock) to each other.

At the release of SYNC (seen by all devices) the transmitter begins ILAS at the next (Tx) LMFC wrap to "0". If F × K has been properly set to be greater than the (transmit encode time) + (line propagation time) + (receiver decode time), received data will propagate out of the receiver's SerDes before the next LMFC. The receiver will pass the data into a FIFO, which will begin outputting data at the next (Rx) LMFC boundary. This "known relationship" between the transmitter's SerDes input and the receiver's FIFO output are known as the "deterministic latency".

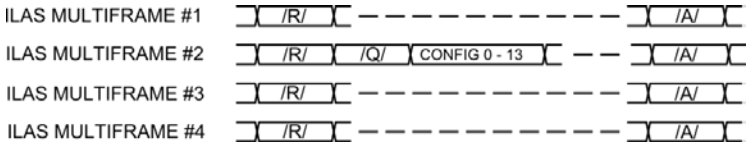

Figure 4. Logic Output of JESD204B Subclass 0 Link Signals During ILAS Phase

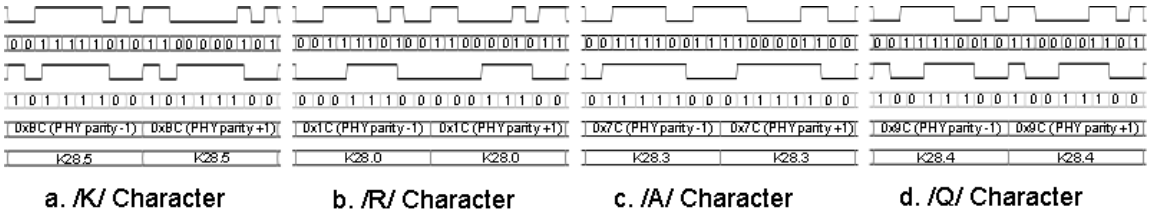

Figure 5. Figure of /K/ Character [K28.5], /R/ Character [K28.0], /A/ Character [K28.3], and /Q/ character [K28.4]

Table 1. Table of CONFIG (Fourteen JESD204B Configuration Parameters Octets) in ILAS Multiframe 2

Octet No.	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	DID[7:0]							
1	ADJCNT[3:0]				BID[3:0]			
2		ADJDIR	PHADJ	LID[4:0]				
3	SCR			L[4:0]				
4	F[7:0]							
5				K[4:0]				
6	M[7:0]							
7	CS[1:0]			N[4:0]				
8	SUBCLASS[2:0]			N[4:0]				
9	JESDV[2:0]			S[4:0]				
10	HD			CF[4:0]				
11	RESERVED 1							
12	RESERVED 2							
13	FCHK[7:0]							

WHAT CAN GO WRONG?

JESD204B can be a complicated interface standard, with many operational subtleties. Finding out why it is not working requires a good understanding of likely scenarios:

Stuck in CGS mode: if SYNC stays at logic low level; or pulse high for <4 multiframes:

1. Checking the board, unpowered:
   a) SYSREF and SYNC~ signaling should be dc coupled.
   b) With the board unpowered, check that the board SYNC~ connections from the SYNC~ source (typically from the FPGA or DAC) to the SYNC~ input (typically ADC or FPGA) are good and low impedance.
   c) Check that the pull-down or pull-up resistors are not dominating the signaling, for example, if values are too small or shorted and, therefore, cannot be driven correctly.
   d) Verify that the differential-pairs traces (and cables, if used) of JESD204B link are matched.
   e) Verify differential impedance of the traces is 100 Ω.
2) Checking the board, powered:
   a) If there is a buffer/translator in the SYNC path, make sure it is functioning properly.
   b) Check that SYNC~ source and board circuitry (both SYNC+ and SYNC–, if differential) are properly configured to produce logic levels compliant for the SYNC~ receive device. If logic level is not compliant, then review circuitry for source and receive configurations to find the problem. Otherwise, consult device manufacturer.
   c) Check that the JESD204B serial transmitter and board circuitry are properly configured to produce the correct logic levels for the JESD204B serial data receiver. If logic level is not compliant review circuitry of source and receive configurations to find the problem. Otherwise, consult device manufacturer.
3) Checking SYNC~ signaling:
   a) If SYNC~ is static and logic low, the link is not progressing beyond the CGS phase. There is either an issue with the data being sent, or the JESD204B receiver is not decoding the samples properly. Verify /K/ characters are being sent, verify receive configuration settings, verify SYNC~ source, review board circuitry, and consider overdriving SYNC~ signal and attempt to force link into ILAS mode to isolate link Rx vs. Tx issues. Otherwise, consult device manufacturer.
   b) If SYNC~ is static and logic high, verify the SYNC~ logic level is configured correctly in the source device. Check pull-up and pull-down resistors.
   c) If SYNC~ pulses high and returns to logic-low state for less than six multiframe periods, the JESD204B link is progressing beyond the CGS phase but not beyond ILAS phase. This would suggest the /K/ characters are okay and the basic function of the CDR are working. Proceed to the ILAS troubleshooting section.
   d) If SYNC~ pulses high for a duration of more than six multiframe periods, the link is progressing beyond the ILAS phase and is malfunctioning in the data phase; see the data phase section for troubleshooting tips.
4) Checking serial data
   a) Verify the Tx data rate and the receiver's expected rate are the same.
   b) Measure lanes with high impedance probe (differential probe, if possible); if characters appear incorrect, make sure lane differential traces are matched, the return path on the PCB is not interrupted, and devices are properly soldered on the PCA. Unlike the (seemingly) random characters of ILAS and data phase, CGS characters are easily recognizable on a scope (if a high enough speed scope is available).
   c) Verify /K/ characters with high impedance probe.
      i) If /K/ characters are correct, the Tx side of the link is working properly.
      ii) If /K/ characters are not correct, the Tx device or the board Lanes signal have an issue.
   d) If dc coupled, verify that the transmitter and receiver common-mode voltage is within specification for the devices
      i) Depending upon implementation, the transmitter common-mode voltage can range from 490 mV to 1135 mV.
      ii) Depending upon implementation, the receiver common-mode voltage can range from 490 mV to 1300 mV.

e) Verify the transmitter CML differential voltage on the data lanes (note that the CML differential voltage is calculated as two times the voltage swing of each leg of the signal).
   i) The transmitter CML differential voltage can range from 0.5 Vpk-pk to 1.0 Vpk-pk for speeds up to 3.125 Gbps.
   ii) The transmitter CML differential voltage can range from 0.4 Vpk-pk to 0.75 Vpk-pk for speeds up to 6.374 Gbps.
   iii) The transmitter CML differential voltage can range from 0.360 Vpk-pk to 0.770 Vpk-pk for speeds up to 12.5 Gbps.

f) Verify the receiver CML differential voltage on the data lanes (note that the CML differential voltage is calculated as two times the voltage swing of each leg of the signal).
   i) The receiver CML differential voltage can range from 0.175 Vpk-pk to 1.0 Vpk-pk for speeds up to 3.125 Gbps.
   ii) The receiver CML differential voltage can range from 0.125 Vpk-pk to 0.75 Vpk-pk for speeds up to 6.374 Gbps.
   iii) The receiver CML differential voltage can range from 0.110 Vpk-pk to 1.05 Vpk-pk for speeds up to 12.5 Gbps.

g) If preemphasis is an option, enable and observe data signals along the data path.

h) Verify that the M and L values match between the transmitter and receiver, otherwise the data rates may not match. For example, M = 2 and L= 2 will expect ½ the data rate over the serial interface as compared to the M = 2 and L = 1 case.

i) Ensure the device clock going to the transmitter and receiver is phase locked and at the correct frequency.

Can not get beyond ILAS mode if SYNC pulses high for approximately four multiframes:

1) Link parameter conflicts
   a) Verify link parameters are not offset by 1 (many parameters are specified as value −1)
   b) Verify ILAS multiframes are transmitting properly, verify link parameters on the Tx device, the Rx device, and those transmitted in ILAS second multiframe.
   c) Calculate expected ILAS length (t_{frame}, $t_{multiframe}$, 4 × $t_{multiframe}$), verify ILAS is attempted for approximately four multiframes.
2) Verify all lanes are functioning properly. Ensure there are no multilane/multilink conflicts.

Get into data phase but occasionally link resets (returns to CGS and ILAS before returning to data phase):

1) Invalid setup and hold time of periodic or gapped periodic SYSREF or SYNC~ signal.
2) Link parameter conflicts.
3) Character replacement conflicts.
4) Scrambling problem, if enabled.
5) Lane data corruption, noisy or jitter could force the eye diagram to close.
6) Spurious clocking or excessive jitter on device clock.

Other general tips when troubleshooting link:

- Run converter and link at slowest allowed speed, as this allows use of lower-bandwidth measurement instruments that are more readily available.
- Set minimum allowed combinations of M, L, K, S.
- Use test modes when possible.
- Use Subclass 0 for troubleshooting.
- Disable scrambling while troubleshooting.

This troubleshooting guide cannot be all inclusive but provides a good basic baseline for an engineer working with and wanting to learn about a JESD204B link.

This summary of the JESD204B specification provides practical information about the link. Hopefully, engineers getting involved with this latest high performance interface standard will find it informative and helpful if troubleshooting is required.

ABOUT THE AUTHOR

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Synchronizing Multiple ADCs Using JESD204B

by Ian Beavers, Applications Engineer, Analog Devices, Inc.

IDEA IN BRIEF

Many communications, instrumentation, and signal acquisition systems require the ability to simultaneously sample analog input signals across multiple analog-to-digital converters (ADC). The sampled data then needs to be processed with the expectation of synchronization across these inputs that each have their own various different latencies. This has historically been a difficult challenge for system designers to meet with LVDS and parallel output ADCs.

JESD204B provides a framework for high speed serial data to be sent along one or more differential signal pairs, such as an output of an ADC. There is an inherent scheme in the interface to achieve coarse alignment across lanes within the JESD204B specification. Data is partitioned into frames with boundaries that are continuously sent to the receiver. The JESD204B Subclass 1 interface has provisions for data alignment down to the sample level across multiple serial lane links or multiple ADCs by using a system reference event signal (SYSREF) to synchronize internal framing clocks in both the transmitter and receiver. This creates a deterministic latency for the devices using the JESD204B link. However, there are still many challenges that a system designer must overcome to achieve full timing closure for sampling synchronization, such as PCB layout considerations, matched clock, and SYSREF generation to meet timing, SYSREF periodicity, and digital FIFO delays.

The designer must decide how the device clock and SYSREF signal will be created and distributed throughout the system. Ideally, the device clock and SYSREF should be of the same swing level and offset to prevent inherent skew at the component input pin. The update rate of the SYSREF event will need to be determined as either a single event at startup or a recurring signal that may occur at any time synchronization is needed. Taking the maximum clock and SYSREF signal skew into consideration, careful PCB layout is needed to meet setup and hold timing across boards, connectors, backplanes, and various components. Finally, digital FIFO design and signals traversing across multiple clock domains create inherent digital buffer skew within JESD204B transmitters and receivers that must be accounted for and removed in back-end data processing.

System clock generation can come from several sources such as crystals, VCOs, and clock generation or clock distribution chips. While the particular system performance will dictate the clocking needs, one, using multiple synchronous ADCs, must be able to produce a SYSREF signal that is source synchronous to the input clock. This makes the clock source selection an important consideration in order to be able to latch this system reference event with a known clock edge at a particular point in time. If the SYSREF signal and clock are not phased locked, this cannot be achieved.

An FPGA can be used to provide a SYSREF event to the system. However, unless it also uses and synchronizes to the master sample clock that is sent to the ADCs, it will be difficult to phase align the SYSREF signal from the FPGA to the clock. An alternate approach is to provide the SYSREF signal from a clock generation or clock distribution chip that can phase align this signal to multiple clocks that are sent throughout the system. Using this method, the SYSREF event can be a one shot event at startup, or a recurring signal depending upon the system requirements.

As long as deterministic latency remains constant within the system across ADCs and FPGAs, additional SYSREF pulses may not be needed except to help frame particular system data. Hence, a periodic SYSREF pulse for clock alignment can be ignored or filtered until the time at which synchronization is lost. A marker sample for the occurrence of SYSREF could alternately be maintained without resetting the JESD204B link.

In order to initiate a known deterministic starting point for the ADC channels, the system engineer must be able to close timing for the SYSREF event signal distributed across the system. This means that the expected setup and hold time, relative to the clock, must be met without violation. Use of a relatively long SYSREF pulse that spans multiple clock cycles can be used to meet the hold time requirement, so long as the setup time to the first required clock can also be met. Careful attention to PCB layout is critical in this effort to maintain matched trace lengths for clocks and SYSREF within the system for minimum skew. This may be the most difficult part of achieving synchronous sampling processing across channels. The effort will only get progressively more

challenging as ADC encode clock rates increase and multiboard systems become more complex.

SYSREF to clock board skew at components across boards and connectors must be deterministically known for each device by the system engineer. Any remaining inter-device digital and clock skew delays need to be effectively nulled in the FPGA or ASIC. Back-end processing can change the sample order across ADCs and introduce any needed re-alignment to prepare the data for further synchronized processing. Correction for inter-device sample skew can be accomplished by delaying the fastest data samples and transmitter latency to align with the slowest data samples in the back-end FPGA or ASIC. For complex systems, this may involve multiple FPGA or ASIC where each needs to communicate their total inter-device sample latency for final alignment. By introducing appropriate elastic buffer delays in the JESD204B receiver(s) to accommodate each specific transmitter latency delay, the inter-device sample skews can be aligned with known determinism across a system.

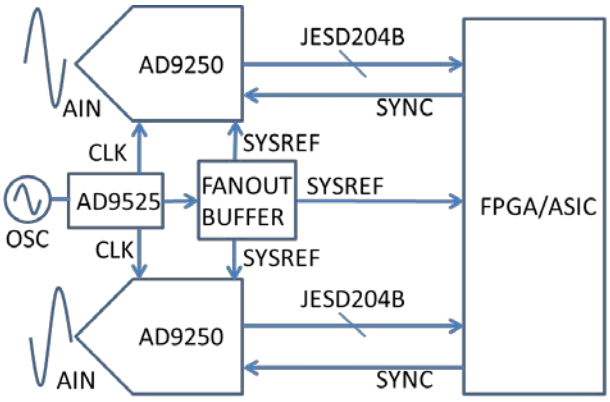

Figure 1. Diagram Showing the AD9250, the AD9525, and FPGA

The AD9250 is a 250 MSPS 14-bit dual ADC from Analog Devices, Inc., that supports the JESD204B interface in a Subclass 1 implementation. This subclass allows analog sample synchronization across ADCs using the SYSREF event signal. The AD9525 is a low jitter clock generator that not only provides seven clock outputs up to 3.1 GHz but is also able to synchronize a SYSREF output signal based on user configurations. These two products, coupled with a selection of fanout buffer products from Analog Devices, provide the framework to accurately synchronize and align multiple ADC data sent to an FPGA or ASIC for processing.

ABOUT THE AUTHOR

Ian Beavers is an applications engineer for the High Speed Converter Group at Analog Devices, Inc. (Greensboro, NC). He has worked for the company since 1999. Ian has over 15 years of experience in the semiconductor industry. He earned a bachelor's degree in electrical engineering from North Carolina State University and an MBA from the University of North Carolina at Greensboro. He can be reached at Ian.Beavers@analog.com.

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Three Key Physical Layer (PHY) Performance Metrics for a JESD204B Transmitter

by Jonathan Harris, Applications Engineer, Analog Devices, Inc.

INTRODUCTION

With the increased adoption of the JESD204 interface in data converters, it has become necessary to devote more attention to the performance and optimization of the digital interface. The focus must not be only on the data converter performance. The first two revisions of the standard, JESD204 in 2006 and JESD204A in 2008, specified data rates of 3.125 Gbps. The latest revision, JESD204B released in 2011, lists three speed grades with the maximum data rate of 12.5 Gbps. These three speed grades are governed by three different electrical interface specifications formulated by the Optical Internetworking Forum (OIF). For data rates up to 3.125 Gbps, OIF-Sx5-01.0, details the electrical interface specifications while the CEI-6G-SR and CEI-11G-SR detail the specifications for data rates up to 6.375 Gbps and 12.5 Gbps, respectively. The high speed data rates require more attention be given to the design and performance of the high speed CML drivers, receivers, and interconnect network which make up the physical interface (PHY) of the JESD204B interface.

To evaluate the performance of the PHY for a JESD204B transmitter, there are several performance metrics that are evaluated. These include common-mode voltage, differential peak-to-peak voltage, differential impedance, differential output return loss, common-mode return loss, transmitter short circuit current, eye diagram mask, and jitter. This article will focus on three key performance metrics that are typically used to evaluate the quality of the transmitted signal, the eye diagram, the bathtub plot, and the histogram plot. These measurements are made from the perspective of the receiver as that is where the signal must be properly decoded. The eye diagram overlays multiple acquisitions of the output data transitions to create a plot that can give many indications of the link quality. This plot can be used to observe many characteristics of the JESD204B physical interface such as impedance discontinuities and improper terminations. This is just one way that the physical layer can be evaluated. The bathtub plot and the histogram plot are two other important performance metrics that are used to evaluate the quality of the JESD204B link. The bathtub plot gives a visual representation of the bit error rate (BER) for a given eye width opening, measured in terms of the unit interval (UI). The unit interval is the specified time given in the physical layer specifications for JESD204B that gives the amount of time between data transitions. The third measurement is the histogram plot which gives the distribution of the measured UI variation. The measurement is also an indication of the amount of jitter present in the measured signal. This plot, along with the eye diagram and the bathtub plot, can be used to gauge the overall performance of the physical layer of the JESD204B interface. A JESD204B transmitter with an output data rate of 5.0 Gbps is presented. The performance for a transmitter of this data rate is detailed by the OIF CEI-6G-SR specification.

THE EYE DIAGRAM

Figure 1 shows an eye diagram for a JESD204B transmitter with a 5.0 Gbps data rate. The ideal waveform is overlaid on a measured waveform. Ideally, the transitions would be almost instantaneous with no overshoot or undershoot and without any ringing. In addition, the cross points which determine the UI would be without jitter. As can be seen from Figure 1, in a real system, ideal waveforms are not possible to achieve due to nonideal transmission media which has loss and terminations that are not matched exactly. The eye diagram shown is a measurement made at the receiver in a JESD204B system. The signal has passed through a connector and approximately 20 cm of differential transmission lines before making it to the measurement point. This eye diagram indicates a reasonable impedance match between the transmitter and receiver and a good transmission media with no large impedance discontinuities. It does exhibit an amount of jitter but not in excess of the specifications for the JESD204 interface. The eye diagram does not exhibit any overshoot but does have a slight amount of undershoot on the rising edges due to the slowing of the signal as it passes through the transmission media. This is to be expected, however, after passing through the connector and the 20 cm of differential transmission lines. The mean UI looks to match the expected UI of approximately 200 ps with the signal having a small amount of jitter. Overall, this eye diagram presents a good signal to the receiver which

should have no trouble recovering the embedded data clock and properly decoding the data.

The eye diagram presented in Figure 2 is measured with the same transmission media used in the measurement for Figure 1, with the exception that the termination impedance is incorrect. The effects can be seen in the increased amount of jitter present in the signal at the crossing points, as well as in the nontransition areas. The overall amplitude is compressed in many of the data acquisitions resulting in an eye diagram that is beginning to close. The degradation will cause an increase in the BER at the receiver and could possibly result in the loss of the JESD204B link at the receiver if the eye closes beyond what the receiver can tolerate.

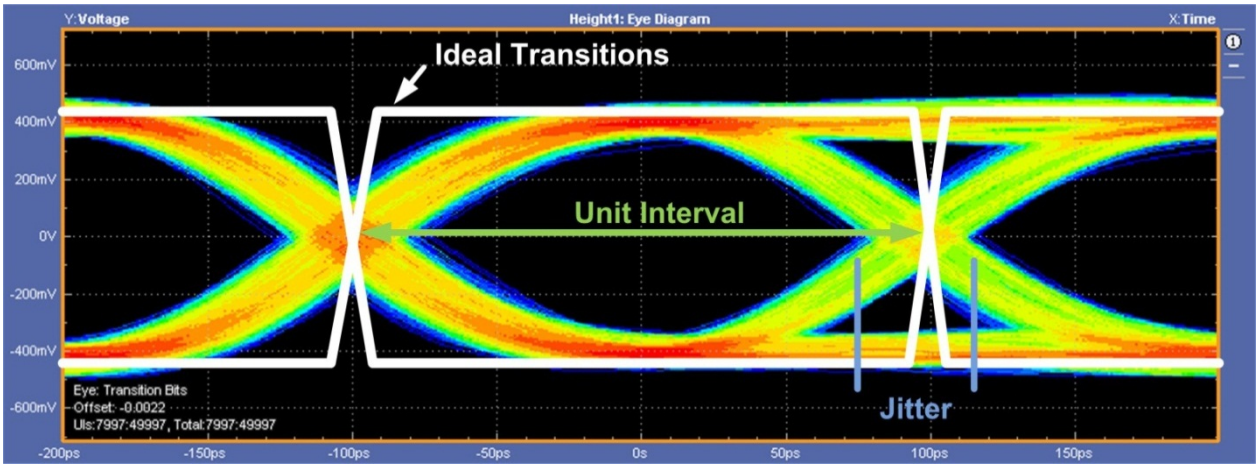

Figure 1. 5.0 Gbps Eye Diagram

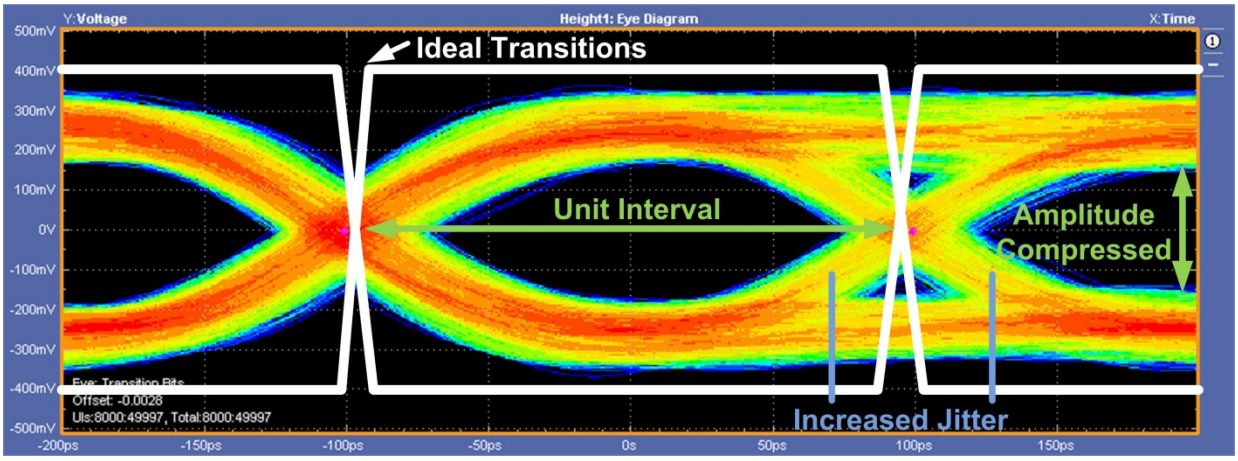

Figure 2. 5.0 Gbps Eye Diagram—Improper Termination

The eye diagram presented in Figure 3 presents another case of a nonideal transmission of data. In this case, an impedance discontinuity is presented at a point midway between the transmitter and the receiver (in this case an oscilloscope). As can be seen by the degraded performance in the plot, the eye opening is closing, meaning that the area inside the transition points is getting smaller. The rising edges and falling edges of the data severely degraded due to the reflections of the impedance discontinuity on the transmission line. The impedance discontinuity also contributes to an increase in the amount of jitter seen at the data transition points. Once the eye closes beyond the limits of the receiver's capability to decode the data stream, the data link will be lost. In the case of Figure 3, it is likely that many receivers would be unable to decode the data stream.

THE BATHTUB PLOT

In addition to the eye diagram, the bathtub plot also provides useful insight into the quality of the serial data transmission on a JESD204B data link. The bathtub plot is a measurement of the BER (bit error rate) as a function of the sampling point as it moves across the eye diagram in time. The bathtub plot is generated by moving the sampling point across the eye diagram and measuring the resultant BER at each point. As Figure 4 illustrates, the closer the sampling point is to the center of the eye, the BER decreases. As the sampling point moves closer to the transition points of the eye diagram, the BER increases. The distance between the two slopes of the bathtub plot at a given BER gives the eye opening at the specified BER (10^{-12} in this case).

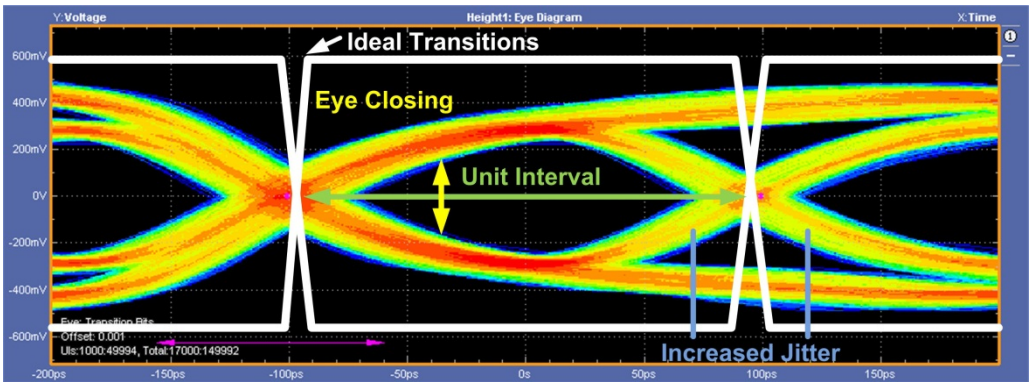

Figure 3. 5.0 Gbps Eye Diagram—Impedance Discontinuity

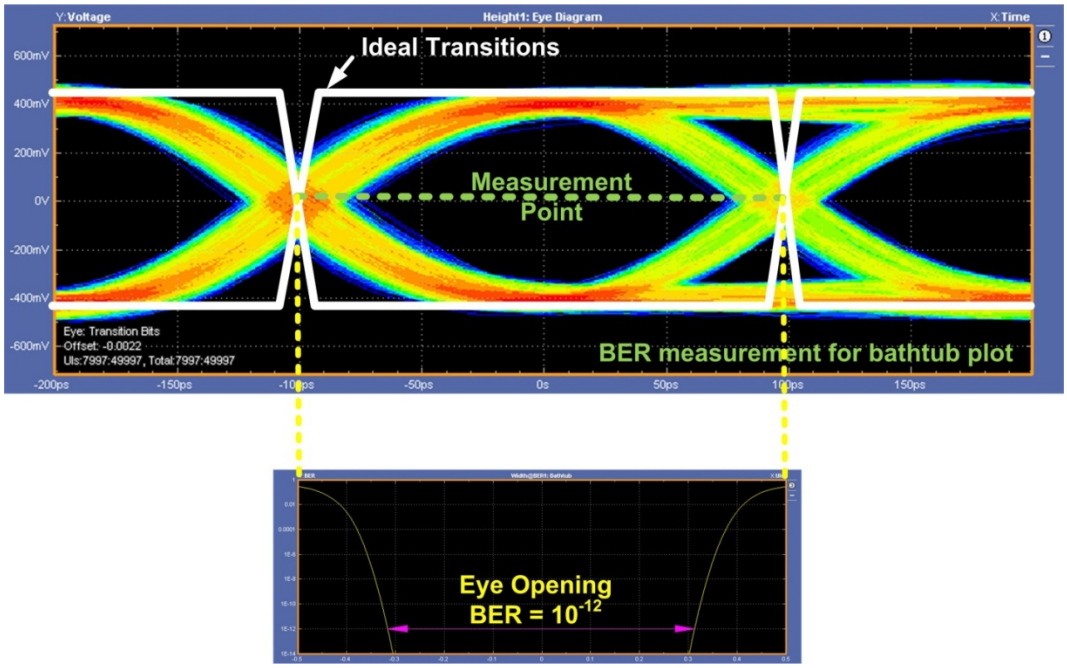

Figure 4. 5.0 Gbps Eye Diagram—Bathtub Plot Measurement

The bathtub plot also provides information on the jitter (Tj) components present in the signal. As Figure 5 shows, when the measurement point is at or near the transition points, it is relatively flat and the main jitter component is deterministic jitter. As with the eye diagram measurements, the bathtub plots are from measurements on a JESD204B 5.0 Gbps transmitter measured at the receiver after passing through a connecter and approximately 20 cm of transmission line. As the measurement point moves closer to the middle of the eye opening, the primary jitter mechanism is random jitter. Random jitter is the result of a large number of processes that are typically small in magnitude. Typical sources would include thermal noise, variations in trace width, shot noise, etc. The PDF (probability density function) of random jitter usually follows a Gaussian distribution. On the other hand, deterministic jitter results from a small number of processes that may have large magnitudes and may not be independent. The PDF of deterministic jitter is bounded and has a well-defined peak-to-peak value. It can have varying shapes and is typically not Gaussian.

An expanded view of the bathtub plot discussed in Figure 4 is given in Figure 6 below. This represents an eye opening of approximately 0.6 UI (unit interval) at the receiver for a 5.0 Gbps serial data transmission with a BER of 10^{-12}. It is important to note that the bathtub plot such as the one in Figure 6 is an extrapolated measurement. The oscilloscope used to capture the data takes a set of measurements and extrapolates the bathtub plot. If one were to use a BERT (bit error rate tester) and acquire enough measurements to build the bathtub plot, it could take hours or even days, even with the high speed operation of today's measurement equipment.

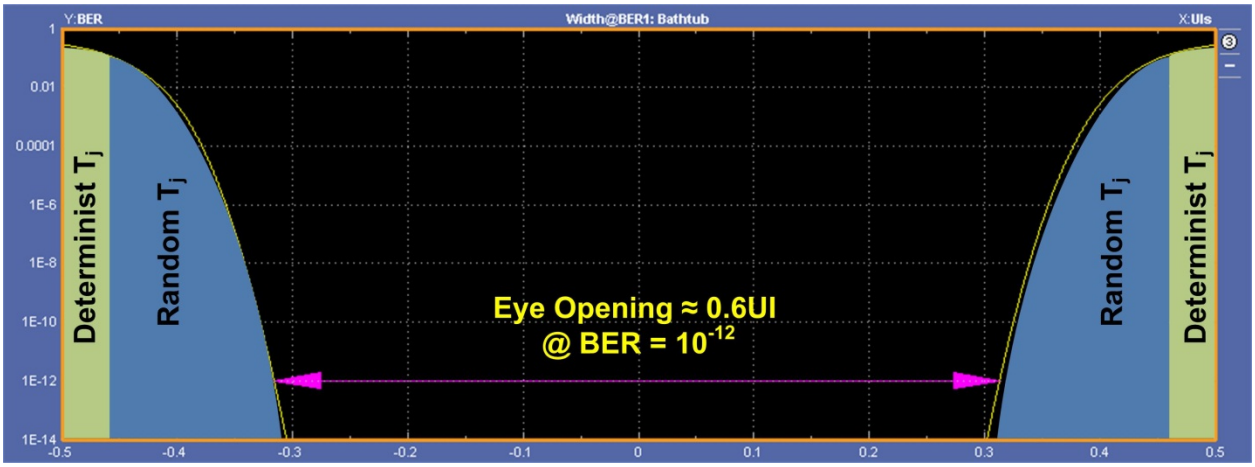

Figure 5. Bathtub Plot—Jitter Components

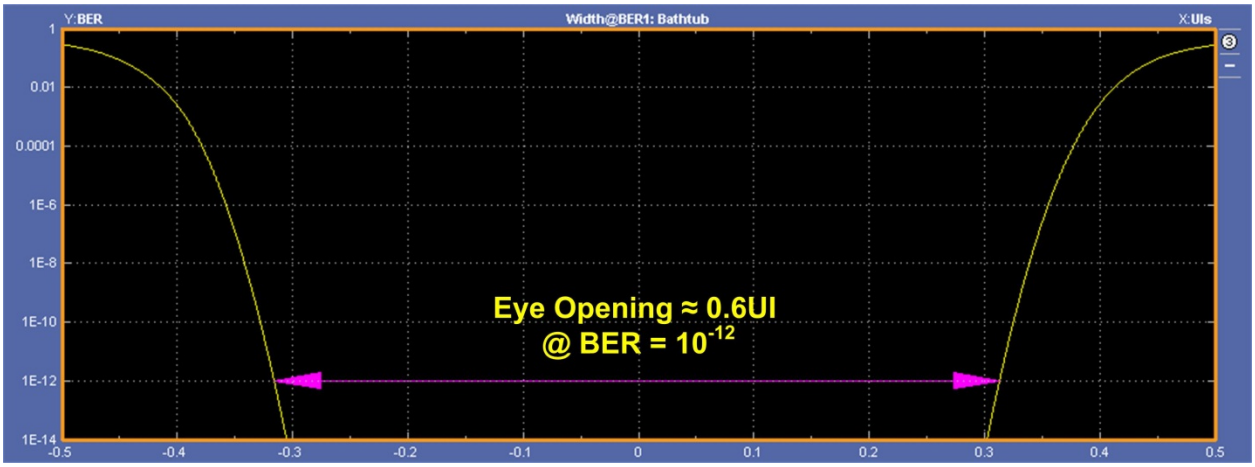

Figure 6. 5.0 Gbps Bathtub Plot

Just as shown in the eye diagram, an improper termination or impedance discontinuity in the system can be seen in the bathtub plot. In contrast to the bathtub plot in Figure 6, the bathtub plots in Figure 7 and Figure 8 exhibit much shallower slopes on each side. The eye opening for a BER of 10^{-12} is only 0.5 UI in both cases which is more than 10% less than the 0.6 UI for the good condition. The improper termination and impedance discontinuity contribute a large amount of random jitter to the system. This is evidenced by the decreasing slope on each side of the bathtub plot along with the decreased eye opening at a BER of 10^{-12}. There is also a small increase in the deterministic jitter as well. This is evidenced again by the decreasing slope near the edges of the bathtub plot.

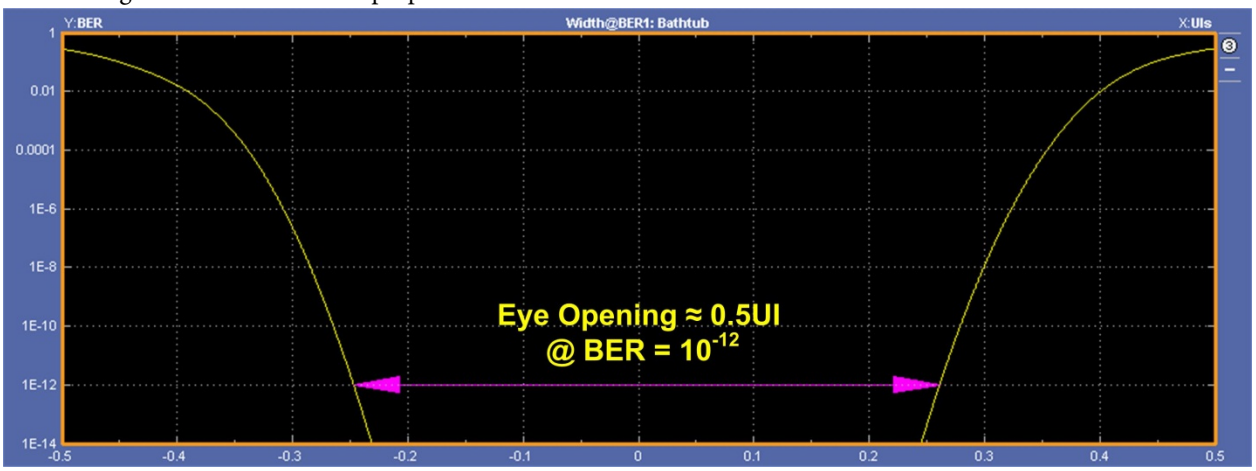

Figure 7. 5.0 Gbps Bathtub Plot—Improper Termination

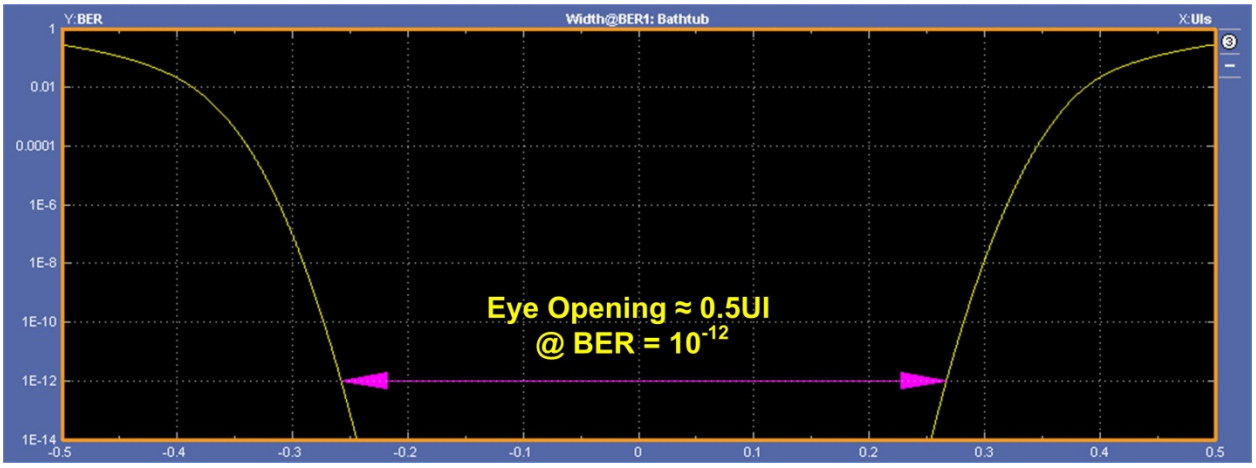

Figure 8. 5.0 Gbps Bathtub Plot—Impedance Discontinuity

THE HISTOGRAM PLOT

A third useful measurement is the histogram plot. This plot shows the distribution of the measured periods between transition points in the data transmission. As with the eye diagram and bathtub plot measurements, the histogram plots are from measurements on a JESD204B 5.0 Gbps transmitter measured at the receiver after passing through a connecter and approximately 20 cm of transmission line. Figure 9 shows a histogram for a relatively good performing system at 5.0 Gbps. The histogram shows a mostly Gaussian type distribution with periods measured between 185 ps and 210 ps. The expected period for a 5.0 Gbps signal should be 200 ps which means the distribution is spread about −7.5% to +5% around its expected value.

When an improper termination is introduced, as shown in Figure 10, the distribution becomes wider and now varies between 170 ps and 220 ps. This increases the percentage of variation from −15% to +10%, which is double that of the measurement shown in Figure 9. These plots show that mostly random jitter is present in the signal since they have a mostly Gaussian-like shape. However, the shape is not exactly Gaussian in nature which indicates there is at least a small amount of deterministic jitter also.

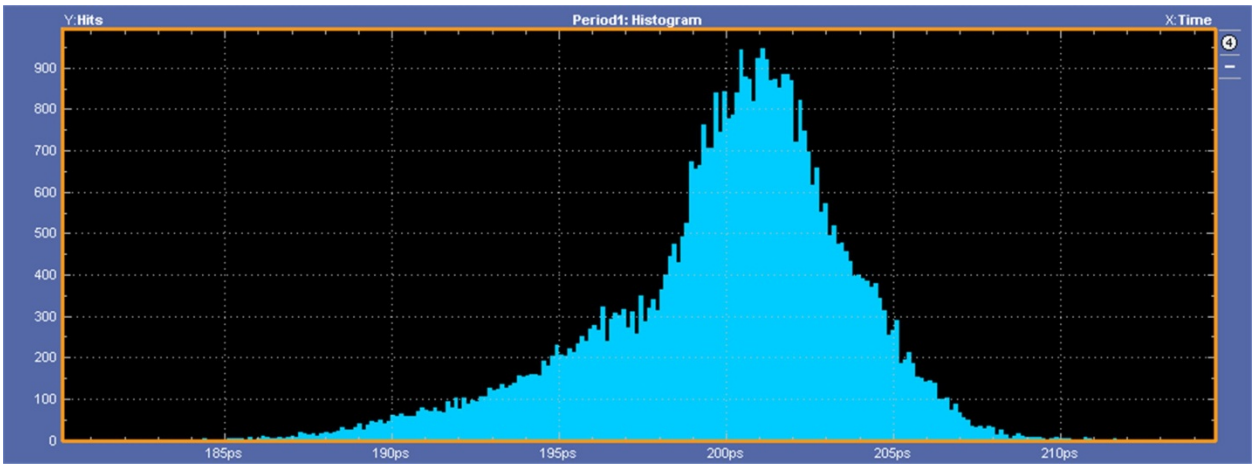

Figure 9. 5.0 Gbps Histogram Plot

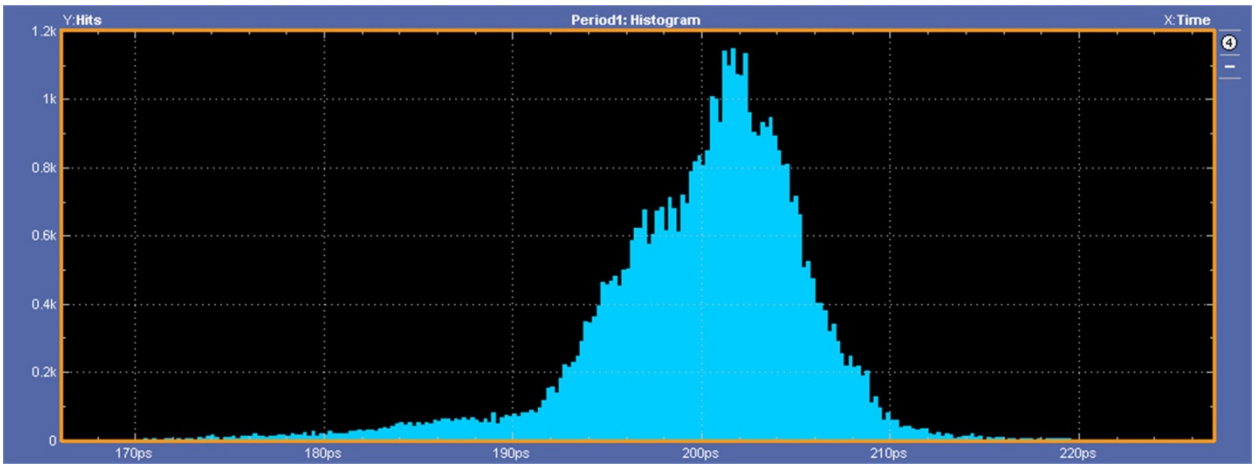

Figure 10. 5.0 Gbps Histogram Plot—Improper Termination

The histogram presented in Figure 11 indicates the results of having an impedance discontinuity along the transmission line. The shape of the distribution is not Gaussian-like at all and has developed a small secondary hump. The mean value of the measured period is also skewed. Unlike the plots in Figure 9 and Figure 10, the mean is no longer 200 ps and has shifted to about 204 ps. The more bimodal distribution indicates that there is more deterministic jitter in the system. This is due to the impedance discontinuity present on the transmission lines and the predictable impacts this has on the system. The range of values measured for the period is again increased, although not as much as in the case of improper termination. In this case, the range is from 175 ps up to 215 ps, which is a range of approximately −12.5% to +7.5% of the expected period. The range isn't as large, but again, the distribution is more bimodal in nature.

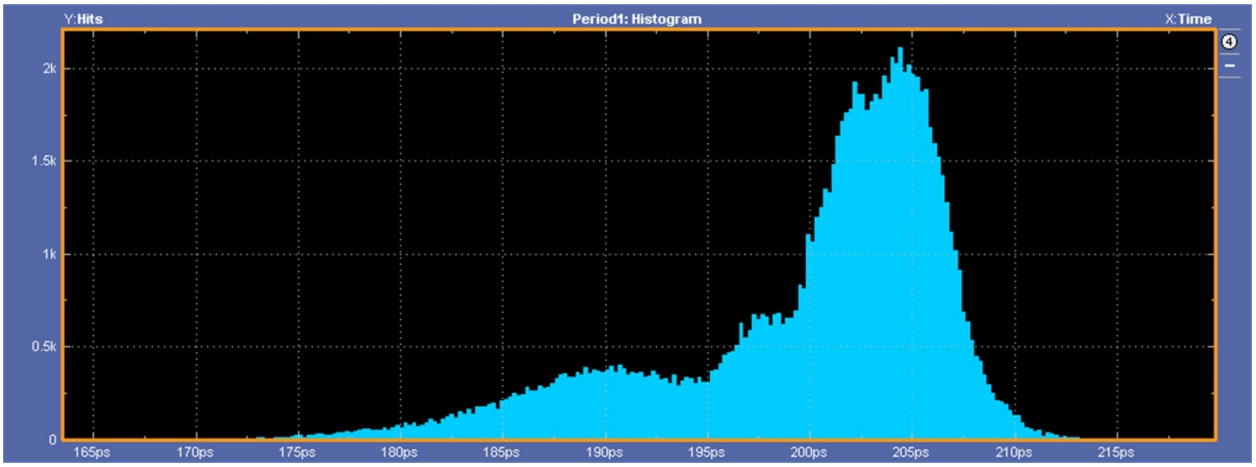

Figure 11. 5.0 Gbps Histogram Plot—Impedance Discontinuity

CONCLUSION

Several performance metrics can be used to evaluate the performance of the physical layer of a JESD204B transmitter. These include common-mode voltage, differential peak-to-peak voltage, differential impedance, differential output return loss, common-mode return loss, transmitter short circuit current, eye diagram mask, and jitter. Three key performance metrics have been discussed that are used to evaluate the quality of the transmitted signal. The eye diagram, bathtub plot, and histogram plot are three important performance metrics that are used to evaluate the quality of the JESD204B link. System issues such as improper terminations and impedance discontinuities have significant impact on the performance of the physical layer. These impacts are evidenced by the degraded performance shown in the eye diagrams, bathtub plots, and histogram plots. It is important to maintain good design practices to properly terminate the system and to avoid impedance discontinuities in the transmission media. These have appreciable negative effects on the data transmission and can result in a faulty data link between the JESD204B transmitter and receiver. Employing techniques to avoid these issues will help to ensure a properly working system.

ABOUT THE AUTHOR

Jonathan Harris is a product applications engineer in the High Speed Converter Group at Analog Devices in Greensboro, NC. He has over seven years of experience as an applications engineer, supporting products in the RF industry. Jonathan received his MSEE from Auburn University and his BSEE from UNC-Charlotte. In his spare time, he enjoys mobile audio, nitro R/C, college football, and spending time with his two children.

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The ABCs of Interleaved ADCs

by Jonathan Harris, Applications Engineer, Analog Devices, Inc.

INTRODUCTION

Across many segments of the market today, interleaving ADCs offers several advantages in many applications. In communications infrastructure there is constantly a push for higher sample rate ADCs to allow for multiband, multicarrier radios, in addition to wider bandwidth requirements for linearization techniques like DPD (digital predistortion). In military and aerospace, higher sample rate ADCs allow for multipurpose systems that can be used for communications, electronic surveillance, and radar just to name a few. In yet another segment, industrial instrumentation, the need is always increasing for higher sample rate ADCs so that higher speed signals can be measured adequately and accurately.

It is first important to understand exactly what interleaving ADCs is about. To understand interleaving, it is good to look at what is actually happening and how it is being implemented. With a basic understanding, the benefits of interleaving can then be discussed. Of course, as many know, there is no such thing as a free lunch, so the challenges of interleaving need to be evaluated and assessed.

ABOUT INTERLEAVING

When ADCs are interleaved, two or more ADCs with a defined clocking relationship are used to simultaneously sample an input signal and produce a combined output signal that results in a sampling bandwidth at some multiple of the individual ADCs. Utilizing ***m*** number of ADCs allows for the effective sample rate to be increased by a factor of ***m***. For the sake of simplicity and ease of understanding, we'll focus on the case of two ADCs. In this case, if two ADCs with each having a sample rate of f_S are interleaved, the resultant sample rate is simply $2f_S$. These two ADCs must have a clock phase relationship for the interleaving to work properly. The clock phase relationship is governed by Equation 1, where ***n*** is the specific ADC and ***m*** is the total number of ADCs.

$$\emptyset_n = 2\pi\left(\frac{n-1}{m}\right) \quad (1)$$

As an example, two ADCs each, with a sample rate of 100 MSPS, are interleaved to achieve a sample rate of 200 MSPS. In this case, Equation 1 can be used to derive the clock phase relationship of the two ADCs and is given by Equation 2 and Equation 3.

$$\emptyset_1 = 2\pi\left(\frac{1-1}{2}\right) = 0\ radians = 0^o \quad (2)$$

$$\emptyset_2 = 2\pi\left(\frac{2-1}{2}\right) = \pi\ radians = 180^o \quad (3)$$

Now that the clock phase relationship is known, the construction of samples can be examined. Figure 1 gives a visual representation of the clock phase relationship and the sample construction of two 100 MSPS interleaved ADCs. Notice the 180° clock phase relationship and how the samples are interleaved. The input waveform is alternatively sampled by the two ADCs. In this case, the interleaving is implemented by using a 200 MHz clock input that is divided by a factor of two and the required phases of the clock to each ADC.

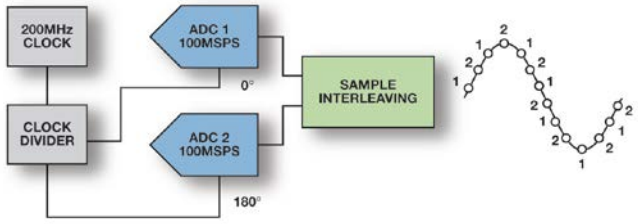

Figure 1. Two Interleaved 100 MSPS ADCs—Basic Diagram

Another representation of this concept is illustrated in Figure 2. By interleaving these two 100 MSPS ADCs, the sample rate is increased to 200 MSPS. This extends each Nyquist zone from 50 MHz to 100 MHz, doubling the available bandwidth in which to operate. The increased operational bandwidth brings many advantages to applications across many market segments. Radio systems can increase the number of supported bands; radar systems can improve spatial resolution, and measurement equipment can achieve greater analog input bandwidth.

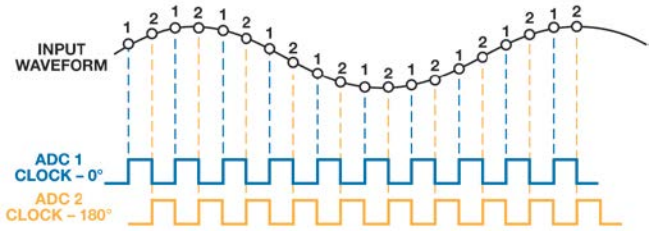

Figure 2. Two Interleaved 100 MSPS ADCs—Clocking and Samples

BENEFITS OF INTERLEAVING

The benefits of interleaving span across multiple segments of the market. The most desired benefit of interleaving is the increased bandwidth made possible by the wider Nyquist zone of the interleaved ADCs. Once again, taking the example of two 100 MSPS ADCs interleaved to create a sample rate of 200 MSPS, Figure 3 gives a representation of the much wider bandwidth allowed by interleaving the two ADCs. This creates advantages for many different applications. As cellular standards increase channel bandwidth and the number of operating bands, there are increased demands on the available bandwidth in the ADC. In addition, in military applications, the requirements for better spatial recognition, as well as increased channel bandwidths in backend communications require higher bandwidths from the ADC. Due to the increased demands for bandwidth in these areas, there is a need created to measure these signals accurately. Therefore, measurement equipment has increased needs for higher bandwidths in order to properly acquire and measure these signals that have higher bandwidth. The system requirements in many designs inherently stay ahead of commercial ADC technology. Interleaving allows for some of this gap to be closed.

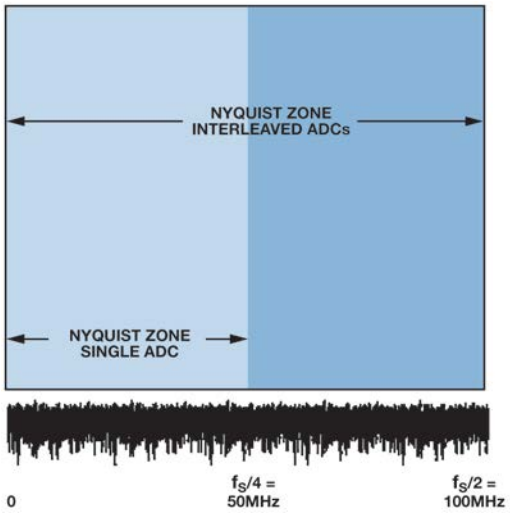

Figure 3. Two Interleaved ADCs—Nyquist Zone

The increased sample rate provides more bandwidth for these applications but also allows for easier frequency planning and reduction in the complexity and cost of the anti-aliasing filter that is typically used at the ADC inputs. With all these great benefits, one has to wonder what the price is to pay. As with most things, there is no such thing as a free lunch. Interleaved ADCs offer increased bandwidth and other nice benefits, but there are some challenges that arise when dealing with interleaved ADCs.

CHALLENGES WITH INTERLEAVING

There are some challenges and things to look out for when interleaving ADCs. There are spurs that appear in the output spectrum that result from the imperfections associated with interleaving ADCs. These imperfections are basically mismatches between the two ADCs that are being interleaved. There are four basic mismatches that result in spurs in the output spectrum. These are offset mismatch, gain mismatch, timing mismatch, and bandwidth mismatch.

The easiest of these to understand is probably the offset mismatch between the two ADCs. Each ADC will have an associated dc offset value. When the two ADCs are interleaved and samples are acquired alternatively back and forth between the two ADCs, the dc offset of each successive sample is changing. Figure 4 gives an example of how each ADC has its own dc offset and how the interleaved output will effectively switch back and forth between these two dc offset values. The output switches between these offset values at a rate of $f_S/2$ which will result in a spur in the output spectrum located at $f_S/2$. Since the mismatch itself does not have a frequency component and is only at dc, the frequency of the spur that appears in the output spectrum only depends on the sampling frequency and will always appear at a frequency of $f_S/2$. The magnitude of the spur is dependent upon the magnitude of the offset mismatch between the ADCs. The greater the mismatch, the larger the spur will be. In order to minimize the spur caused by the offset mismatch, it is not necessary to completely null the dc offset in each ADC. Doing this would filter out any DC content in the signal and would not work for systems using a ZIF (zero IF) architecture where the signal content is real and complex and includes data at DC. Instead, a more appropriate technique would be to match the offset of one of the ADCs to the other ADC. The offset of one ADC is chosen as the reference, and the offset of the other ADC is set to match that value as closely as possible. The better matched the offset values are, the lower the resulting spur is at $f_S/2$.

The second mismatch to look at when interleaving is the gain mismatch between the ADCs. Figure 5 gives a representation of the gain mismatch between two interleaved converters. In this case, there is a frequency component to the mismatch. In order to observe this mismatch, there has to be a signal applied to the ADCs. In the case of the offset mismatch, no signal is necessary to see the inherent dc offset of the two ADCs. In the case of the gain mismatch, there is no way to see the gain mismatch unless a signal is present and the gain mismatch can be measured. The gain mismatch will result in a spur in the output spectrum that is related to the input frequency, as well as the sampling rate, and will appear at $f_S/2 \pm f_{IN}$. In order to minimize the spur caused by

the gain mismatch, a similar strategy as what is used for the offset mismatch is employed. The gain of one of the ADCs is chosen as the reference, and the gain of the other ADC is set to match that gain value as closely as possible. The better the gain values of each ADC are matched to each other, the less the resulting spur will be in the output spectrum.

Next, we must examine the timing mismatch between the two ADCs. The timing mismatch has two components, group delay in the analog section of the ADC and clock skew. The analog circuitry within the ADC has an associated group delay and the value can be different between the two ADCs. In addition, there is clock skew that has an aperture uncertainty component in each of the ADCs and has a component related to the accuracy of the clock phases that are input to each converter. Figure 6 gives a visual representation of the mechanism and effects of the timing mismatches in the ADCs. Similar to the gain mismatch spur, the timing mismatch spur is also a function of the input frequency and the sample rate and appears at $f_S/2 \pm f_{IN}$. In order to minimize the resulting spur, the group delay through the analog section of each converter needs to be properly matched with good circuit design techniques. In addition, the clock path designs need to be closely matched to minimize aperture uncertainty differences. And lastly, the clock phase relationships need to be precisely controlled such that the two input clocks are as close to 180° apart as possible. As with the other mismatches, the goal is to attempt to minimize the mechanisms that cause the timing mismatch.

The last mismatch to look at is probably the most difficult to comprehend and handle; it is the bandwidth mismatch. As shown in Figure 7, the bandwidth mismatch has a gain and a phase/frequency component. This makes bandwidth mismatch more difficult because it contains components from two of the other mismatch parameters. In the bandwidth mismatch, however, we see different gain values at different frequencies. In addition, the bandwidth has a timing component which causes signals at different frequencies to have different delays through each converter. The best way to minimize the bandwidth mismatch is to have very good circuit design and layout practices that work to minimize the bandwidth mismatches between the ADCs. The better matched each ADC is, the less the resulting spur will be. Just as the gain and timing mismatches caused spurs in the output spectrum at $f_S/2 \pm f_{IN}$, the bandwidth mismatch also results in a spur at the same frequency.

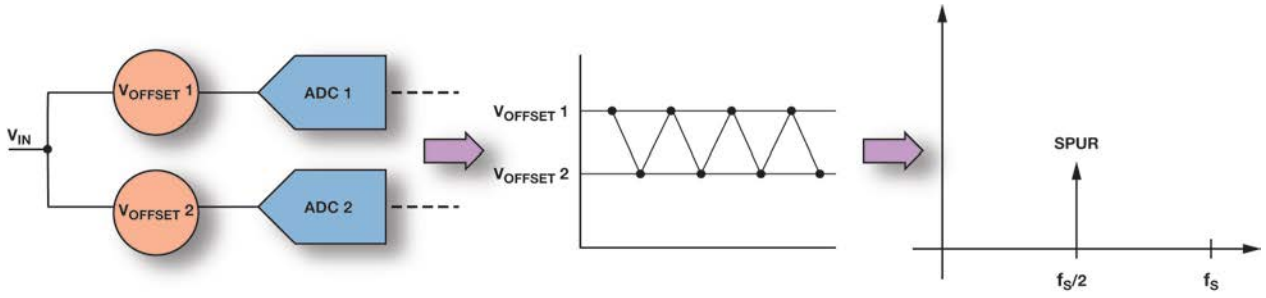

Figure 4. Offset Mismatch

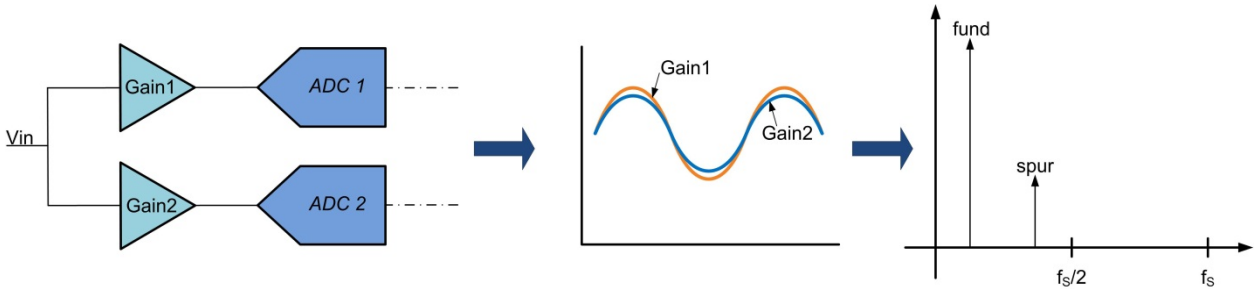

Figure 5. Gain Mismatch

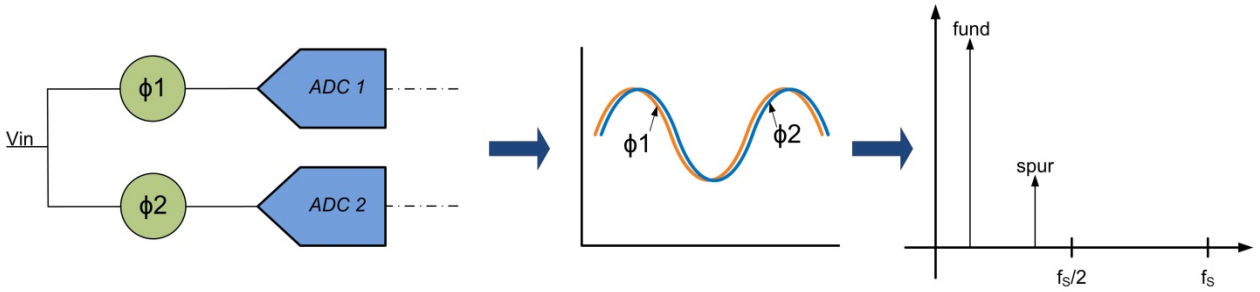

Figure 6. Timing Mismatch

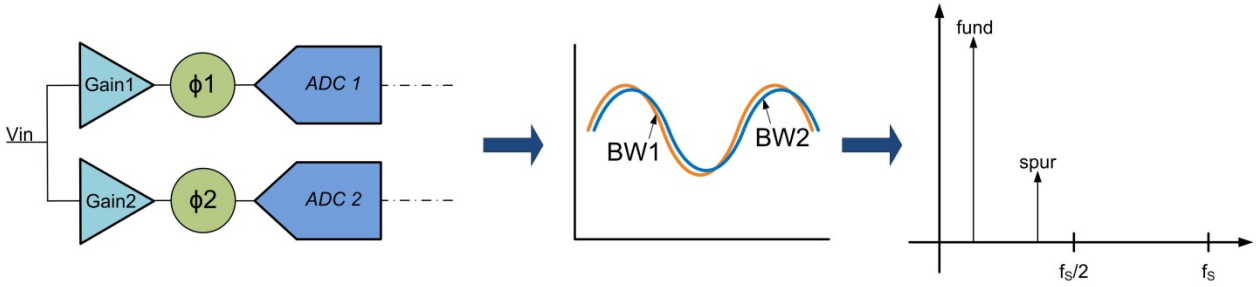

Figure 7. Bandwidth Mismatch

Now that we've discussed four different mismatches that cause issues when interleaving ADCs, it is apparent that a commonality has emerged. Three of the four mismatches produce a spur in the output spectrum at $f_S/2 \pm f_{IN}$. The offset mismatch spur can be easily identified since it alone resides at $f_S/2$ and can be compensated fairly easily. The gain, timing, and bandwidth mismatches all produce a spur at $f_S/2 \pm f_{IN}$ in the output spectrum so the question is how to identify the contribution of each. Figure 8 gives a quick visual guide to the process of identifying the sources of the spurs from the different mismatches of interleaved ADCs.

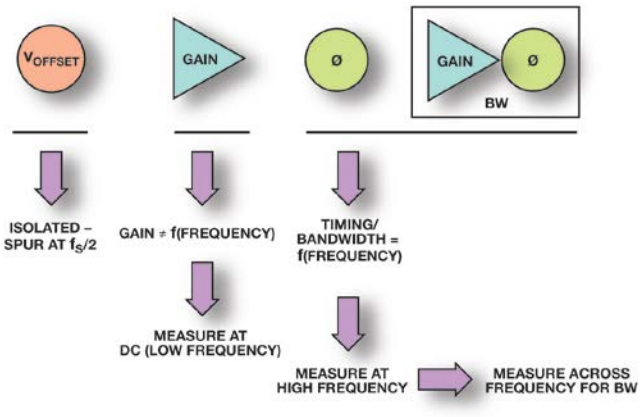

Figure 8. Interrelated Nature of Interleaving Mismatches

If looking purely at gain mismatch alone, it is a low frequency, or dc, type of mismatch. The gain component of the bandwidth mismatch can be separated from the gain mismatch by performing a gain measurement at low frequency near dc and then performing gain measurements at higher frequencies. The gain mismatch is not a function of frequency like the gain component of the bandwidth mismatch. A similar approach is used for the timing mismatch. A measurement is performed at low frequency near dc and then subsequent measurements are performed at higher frequencies to separate the timing component of bandwidth mismatch from the timing mismatch.

CONCLUSION

The newest communication system designs, cutting edge radar technologies, and ultrahigh bandwidth measurement equipment seem to constantly outpace the available ADC technology. These requirements push both users and manufacturers of ADCs to develop methods to keep pace with these demands. Interleaving ADCs allows for greater bandwidths to be achieved at a faster pace than the traditional path of increasing the conversion rate of a typical ADC. By taking two or more ADCs and interleaving them together, the available bandwidth is increased, and system design requirements can be met at a faster pace. Interleaving ADCs does not come for free, however, and mismatches between the ADCs cannot be ignored. Even though the mismatches do exist, knowing about them and how to appropriately deal with them can enable designers to use these interleaved ADCs more intelligently and meet the ever increasing demands of their latest system designs.

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TA11329-0-1/13

New, Faster JESD204B Standard for High Speed Data Converters Comes with Verification Challenges

by Frank Farrelly, Product Engineering Manager, Analog Devices, Inc., and Chris Loberg, Senior Technical Marketing Manager, Tektronix

IDEA IN BRIEF

JESD204B is a new 12.5 Gb/s serial interface standard for high speed, high resolution data converters. Already, devices from converter manufacturers are beginning to make their way into the market, and it is expected that the number of JESD204B-enabled products will increase tremendously in the near future. The primary value of the JESD204B interface is a reliable increase in the data transfer bandwidth between a converter and a logic device (such as an FPGA or ASIC).

As with any new interface, JESD204B brings new challenges. For system developers, the challenges are how to best implement JESD204B from a PCB design standpoint and how to debug a system if something isn't initially working right. For component manufacturers, challenges involve testing new JESD204B devices. Testing not only ensures that specifications are being met in a relatively ideal environment, but it also ensures successful JESD204B operation in end system environments.

This article discusses the JESD204B specification, reviews the tesets needed to validate JESD204B devices, and outline methods used to replicate end system environments.

JESD204B—A NATURAL EVOLUTION FOR DATA CONVERTERS

Data converters (digital-to-analog and analog-to-digital) are used in many applications ranging from audio and music to test instrumentation. The world of data converters is evolving. As the bit depth and sample rate go up, it is becoming more and more difficult to get data in and out. A decade or two ago, with sample rates for high speed converters limited to 100 MSPS and below, using TTL or CMOS parallel data busses was sufficient. For example, a 12-bit converter with 12 pins dedicated to the data could be implemented with reasonable setup and hold times with respect to the clock.

As speeds increased above 100 MSPS, setup and hold times for single-ended signals could no longer be maintained. To boost speeds, high speed converters moved to differential signaling but at the cost of increased pin counts. For example, a 12-bit converter now would need 24 pins dedicated to data. To address the pin count issue, serial data interfaces were adopted. A converter data interface with 6× serialization now allows that same 12-bit converter to transfer the data with just two differential I/Os (only four pins). Fast forwarding to today, data converters are now being developed using the JESD204B specification for the data interface.

The JEDEC standards organization has published two versions of the JESD204 high speed serial digital interface specification. The first version, the JESD204 2006 specification, brought the advantages of SerDes-based high speed serial interfaces to data converters with a 3.125 Gbps maximum speed rating. It was revised in 2008, (JESD204A 2008 specification) and added important enhancements including support for multiple data lanes and lane synchronization. The second version of the specification, JESD204B, was developed by an international JEDEC JC-16 task group (Project 150.01), comprised of about 65 members from 25 companies. It provided a number of major enhancements including a higher maximum lane rate, support for deterministic latency through the interface, and support for harmonic frame clocking.

LACK OF AN OFFICIAL COMPLIANCE TEST SPECIFICATION

Unlike many other high speed serial interface standards, the JESD204B standard does not include an official compliance test specification. A test specification is doubly valuable because it lists the tests which must be performed to ensure compatibility, as well as the procedures for doing those tests. Having consistent procedures used by different manufacturers help ensure a common understanding of the specification and eliminate differences in assumptions. The lack of an official compliance test specification does not mean that all is lost. All of the information needed to develop a set of tests and procedures can be found in the JESD204B specification and the specifications it refers to. It is left up to the individual chip manufacturers and system developers to pull together that information.

PHYSICAL LAYER TESTING

Physical layer, or PHY, tests are related to the individual data lane driver and receiver circuitry: in other words, the analog tests of a link. They do not include digital functionality or procedural tests. Working toward the goal of developing a thorough list of PHY tests, a list of recommended SerDes PHY tests can be obtained from the OIF-CEI-02.0 specification, Section 1.7. The JESD204B specification closely follows those recommendations but does include a few modifications. For example, JESD204B does not specify random jitter as a standalone test item, rather choosing to include it under total jitter. Also, JESD204B specifies JSPAT, JTSPAT, and modified RPAT as recommended test patterns, whereas the OIF-CEI-02.0 specifies using the PRBS31 pattern.

Above and beyond the required PHY tests, there are additional PHY tests that could be performed which are not listed in the OIF-CEI-02.0 specification or in the PHY section of the JESD204B specification. One can look to other SerDes compliance test specifications for examples and find tests such as intrapair skew (for a Tx) and intrapair skew tolerance (for an Rx). In bringing these up, it is not the intention to recommend that these tests be added to the JESD204B specification. Additional PHY tests are not required to ensure JESD204B compatibility. The intention is to note that if a particular PHY test is failing, other PHY tests can be used to help gain insight as to why.

Once the list of tests is set, limits for those tests can be obtained from the JESD204B specification. Just keep in mind that there are three sets of limits: LV-OIF-11G-SR, LV-OIF-6G-SR, and LV-OIF-SxI5. A particular JESD204B device may support more than one set of limits. In that case, the component should be tested against all of the sets of limits that are supported.

One point of potential confusion with JESD204B PHY testing is jitter terminology. The JESD204B and OIF-CEI-02.0 specifications use different terminology from what the test equipment vendors use. The typical jitter map is shown in Figure 1. Test equipment makers base their terminology on the industry standard dual Dirac jitter model. This difference in terminology is a point of potential problems in test procedures, as jitter is quite a tricky topic. Table 1 shows our translation of the jitter terminology (the JESD204B specification uses different terminology for jitter from that used by test equipment vendors).

Table 1. Jitter Terms Translation

JESD204B Jitter Term	JESD204B Jitter Name	Test Equipment Jitter Translation
T_UBHPJ	Transmit uncorrelated bounded high probability jitter	BUJ (PJ and NPJ)
T_DCD	Transmit duty cycle distortion	DCD
T_TJ	Transmit total jitter	TJ
R_SJ-HF	Receive sinusoidal jitter, high frequency	PJ > 1/1667 × BR
R_SJ-MAX	Receive sinusoidal jitter, maximum	PJ < 1/166,700 × BR
	Receive bounded high probability jitter—correlated	DDJ
R_BHPJ	Receive bounded high probability jitter—uncorrelated	NPJ
R_TJ	Receive total jitter	TJ

Figure 1. Typical Jitter Map, Including Identification of Bounded Uncorrelated Jitter (BUJ)

Another point of potential confusion with JESD204B PHY testing is the eye mask for data rates above 11.1 Gbps. The JESD204B specification says that for data rates greater than 11.1 Gbps to use a normalized bit time of 11.1 Gbps. So, if running at 12.5 Gbps (with an 80 ps bit period), it says to use the bit period for 11.1 Gbps (90.9 ps). The issue at hand here is that eye masks can be built by starting either at the edge of the UI or from the center of the UI, and the JESD204B does not clearly state which reference point to start from. If the reference point is the center of the UI, then the eye mask is bigger than normal at 12.5 Gbps, making it harder for a Tx to pass but easier for an Rx to work. If the reference point is the edge of the UI, then the eye mask is smaller than normal at 12.5 Gbps, making it easier for a Tx to pass but hard for an Rx to work. Ultimately, until this question is resolved, it is recommended to test against each of the two mask options in order to ensure compatibility.

TIMING TESTING

Coming up with a thorough list of timing tests for JESD204B is not an easy task. There are at least dozen timing diagrams throughout the specification, and it's not immediately apparent which apply to the Tx, the channel, or the Rx. Also, some are only applicable to a particular subclass (0, 1, or 2). An official compliance test specification would be especially helpful here if it were to simply consolidate the timing specifications into a single table. Once time is taken to methodically go through the timing specifications, there is no confusion about them.

One nice thing about timing for system developers is that specifying timing for a JESD204B component turns out to be easier than is immediately apparent from the specification. For Subclass 0 and 2, only Device Clock-to-SYNC~ timing must be specified. For Subclass 1, only Device Clock-to-SYSREF timing must be specified.

PROTOCOL TESTING

As with the PHY tests, there is no official list of JESD204B protocol tests. Therefore, it is left to each user to scour through the specification and compile a list of functions to test. This section lists many of the suggested protocol tests and briefly describes them.

One category of protocol tests are the test sequences. For PHY testing, JESD204B transmitters must be able to output JSPAT and modified RPAT patterns. From a protocol standpoint, there's a need to validate that those patterns are correct. The same is true with JESD204B receivers and the JTSPAT pattern. Optionally, if they support PRBS patterns, those need to be validated as well. Next, are the short and long transport layer patterns. These are included to help system developers debug their systems by proving that the

link is working correctly through the transport layer. From a component manufacturer standpoint, those transport layer patterns have to be validated for every mode of operation that the device supports, which, considering the number of link configuration variables, ends up being a lot of cases.

One question that comes up regarding protocol testing is how to do it at 12.5 Gbps. One recommended solution is to use a high speed oscilloscope with a serial data decoder. Many higher end oscilloscopes are now equipped with a dedicated trigger chip for triggering on 8b/10b data such as that used in JESD204B. Figure 3 shows serial decode of a JESD204B data lane at 6 Gb/s at the beginning of the initial lane alignment sequence (ILAS) sequence.

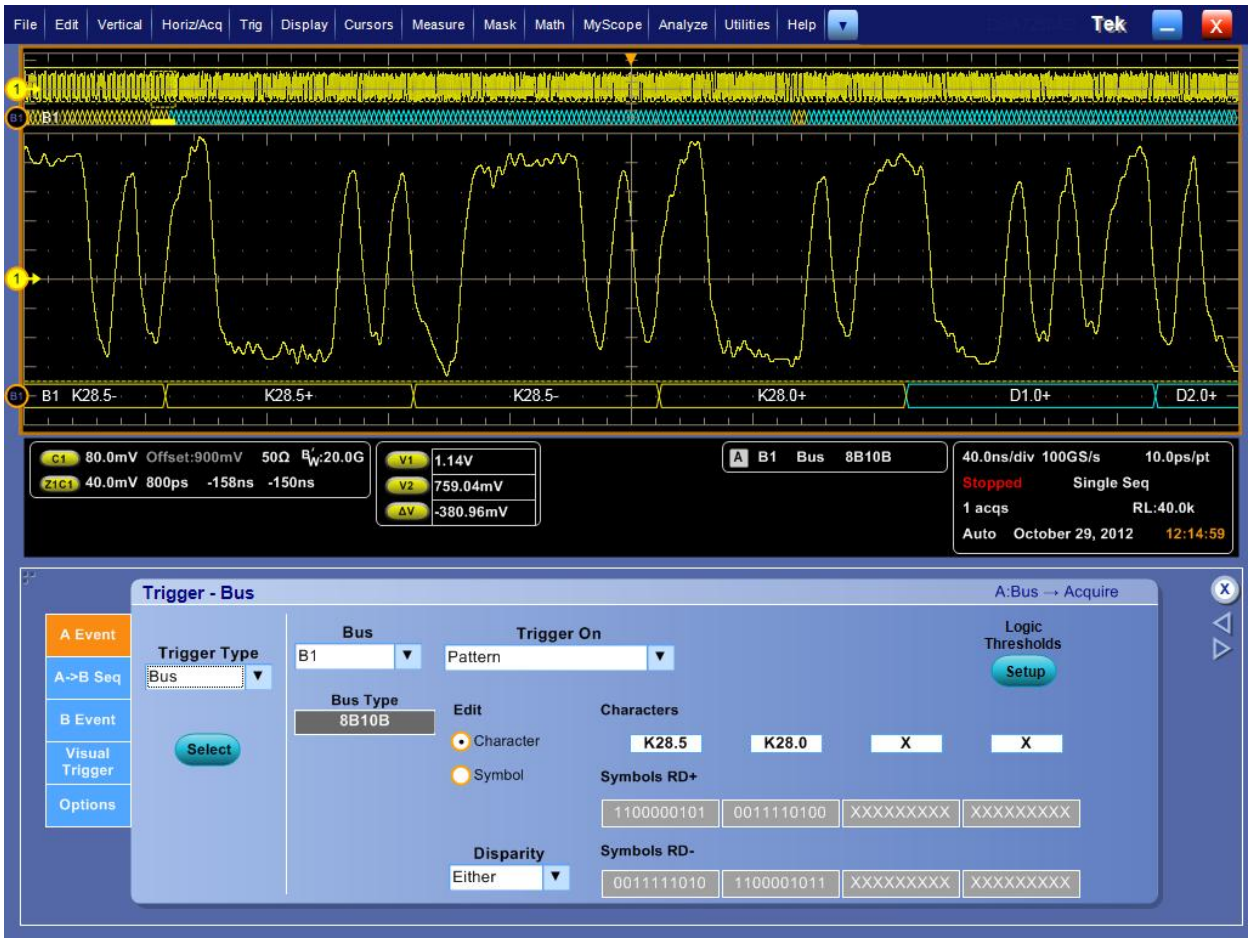

Figure 2. Serial Decode of a JESD204B Data Lane at 6 Gbps Showing the Beginning of the ILAS Sequence

Another group of protocol tests can be built around the ILAS. The ILAS as a whole is fairly complex, so breaking it down into its individual components can make protocol testing more meaningful. The following are some examples of tests that can be measured on a transmitter to validate its operation. Is the multiframe length correct? Does each multiframe start with an /R/ control code and end with an /A/ control code? Is the /Q/ control code in the right location? Is the link configuration data correct and in the right location? The ILAS contains data; is that correct? How many multiframes does the ILAS last? Is the ILAS the same on all lanes? Clearly, there is a lot of potential for protocol testing around the ILAS sequence.

JESD204B does not have a lot of handshaking, but what it does have can be tested. Depending on the subclass, a number of tests can be performed. Since the SYNC~ signal can be used for initial handshaking, error reporting, and link reinitialization, do the Tx and Rx components do their part accordingly? Does the Rx assert SYNC~ starting at the right time and for the right duration? Does the Tx react correctly based on the duration of SYNC~ assertion? Since the data sent over the link also plays a part in the handshaking (i.e., the ILAS), is it correct for its content and with respect to SYNC~ timing?

Next, there are a number of smaller digital functions that need to be tested as part of protocol, including scrambling, 8b/10b encoding/decoding, skew and skew tolerance, control bits, tail bits, SYNC~ signal combining, frame alignment monitoring, and correction. All of these functions need to be validated.

Lastly, there is the category of protocol tests called error handling. The specification includes a minimum set of errors that must be detected and reported: disparity errors, not-in-table errors, unexpected control character errors, and code group synchronization errors. But, there are many more potential errors that could be detected and reported. For each and every type that is detectable by a JESD204B component, there should be a protocol test. These types of protocol tests can be a bit of a challenge to test and validate because a properly working link will never exercise them. They generally will require specialized test equipment. A BERT pattern generator can be used for many tests by creating a pattern that includes an error. Errors cases can also be generated using an FPGA with code modified to specifically generate those errors.

EMPHASIS AND EQUALIZATION TESTING

The JESD204B specification talks very little about emphasis and equalization. There are a few comments like "pre-emphasis might be required" and "equalization might need to be implemented," from which one can determine that the specification allows them but does not give any additional guidance. When using a converter with JESD204B that includes emphasis or equalization, how does one go about determining whether or not to turn it on and if so how much to turn it on? To answer that question, it is first best to understand the type of jitter called intersymbol interference (ISI). ISI is the name for the variation in edge timing that is caused by the filtering effects of a transmission line. Mathematically, it can be simply modeled as a low-pass filter. When sending high speed serial data down a transmission line, the filtering results in a distorted signal. Emphasis and equalization counteract the filtering effects of ISI with the goal of bringing the frequency response at the end of the channel back to as close to flat over frequency as possible and thus, resulting in a signal that is not distorted by ISI.

With a basic understanding of emphasis and equalization and ISI, the next step is setting them. What many people ask first is how long of a trace can be driven with and without emphasis/equalization. Real-world PCB designs have too many variables that can affect ISI to be able to specify the channel in terms of trace length. Variables like trace width, trace length, vias vs. no vias, dielectric material, connectors vs. no connectors, trace material, corners, passive components, and distance to ground plane can all affect channel performance. So, how can channel characteristics ever be correlated to emphasis/equalization? The solution is to specify the channel in terms of insertion loss. Insertion loss is described in the JESD204B specification as a measure of the power loss of a signal over frequency. Emphasis, equalization, and PCB channel can all be related in terms of insertion loss (and gain). Using a relevant frequency (the JESD204B specification lists ¾ baud rate) and an insertion loss limit (JESD204B lists −6 dB), the gain provided by emphasis and/or equalization can be selected to bring the frequency response at the selected frequency up above the loss limit. For example, a PCB channel with −12 dB of loss at +9 GHz would need +6 dB of emphasis/equalization gain to bring the total back up to −6 dB.

Alternately, converters manufacturers can provide a table of emphasis/equalization settings vs. PCB insertion loss. This method can result in a better solution, as it does not depend on as many assumptions. To build such a table for a transmitter (and to emulate end system designs), a set of test evaluation boards can be built with varying trace lengths.

The eye diagram at the end of the PCB trace can be directly measured and compared against the JESD204B Rx mask. By trying various PCB trace lengths, there will be one that results in the eye just barely passing the Rx mask. Since the insertion loss of that specific trace can be measured, the drive capability for a specific emphasis setting is known. Compare Figure 3 showing an eye diagram at the end of an ISI PCB to Figure 4, the eye diagram going into an ISI PCB. In this case, the data rate is 5 Gb/s, the ISI PCB has 8 dB of insertion loss at 4 GHz, and emphasis is off.

Repeating this process vs. emphasis settings will result in a table of emphasis settings vs. insertion loss. A similar approach can be done on a receiver with equalization. Start with a BERT generator that is outputting the maximum allowed total jitter (except for ISI jitter). Using the same set of ISI test boards with varying trace lengths, test with longer and longer traces until the receiver starts to get errors that exceed the target bit error rate (1E-15). Measure the insertion loss of the PCB trace. Repeat for every equalizer setting. In summary, if a JESD204B device manufacturer provides only emphasis/equalization gain, the first method can be used to pick settings. The best method is if the manufacturer provides a table of settings vs. channel insertion loss.

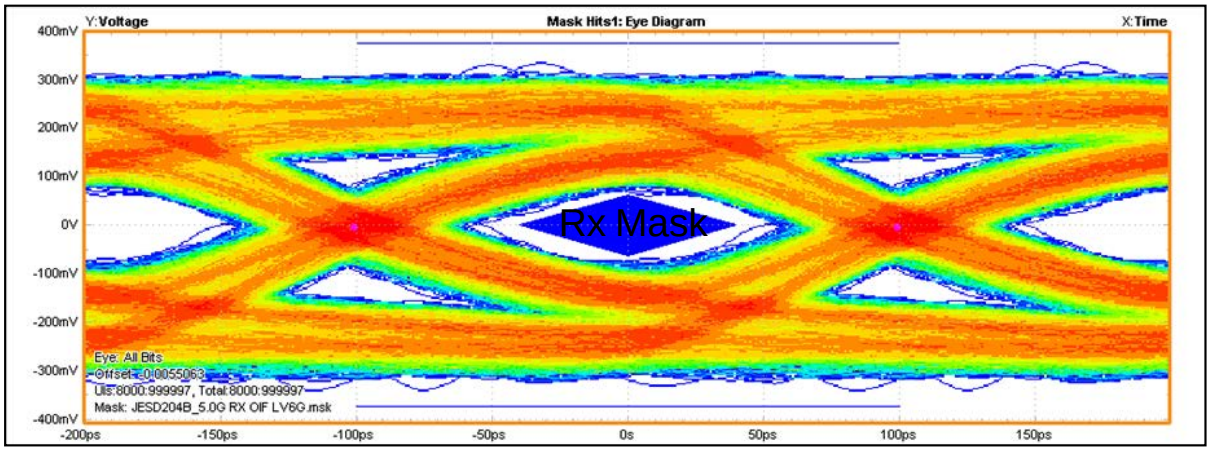

Figure 3. Eye Diagram at the End of a Long ISI PCB

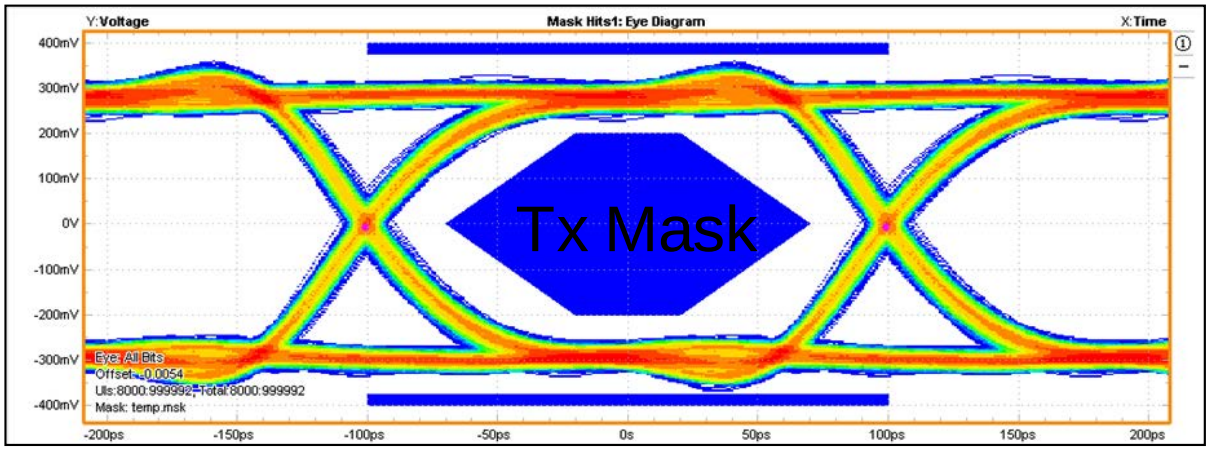

Figure 4. Eye Diagram Going into a Long ISI PCB

Should emphasis or equalization be used? From a frequency response correction standpoint, there's no clear reason to use one or the other. However, in most cases, emphasis can generate a certain amount of gain with less power. If system power is important, that could be a reason to choose emphasis over equalization. Another advantage of choosing emphasis over equalization is that the effect on the signal can be directly measured with an oscilloscope.

It can be common to have both a JESD204B Tx with emphasis and an Rx with equalization. How would you determine when to turn on both? Simply, if the insertion loss of the channel cannot be overcome by just emphasis or just equalization, then it's time to turn on both. As for how much gain to set each of them to, one advantage of specifying response in terms of insertion loss (and gain) is that it's additive. (For example, at the frequency of interest: a PCB trace with −20 dB of loss, a Tx with +6 dB of emphasis, and an Rx with +8 dB of equalization can be represented as −20 dB +6 dB +8 dB = −6 dB total).

EMULATING SYSTEM ENVIRONMENTS—NOISE AND JITTER

No end system design is free of noise and jitter. Emulating system jitter is fully specified in the JESD204B specification, but voltage noise is not. To emulate voltage noise in end system designs, component manufacturers can perform noise tolerance tests. One such test is power supply noise tolerance. For this test, noise is injected onto the components' various power supply domains. The amplitude of the noise is increased until the first compliance tests fails (often the first test to fail on a SerDes will be jitter). This test is repeated over the frequency range at which PCB noise is typically present (a few Hz to around 100 MHz). A plot of maximum power supply noise tolerated vs. frequency is generated. The same test can be performed on all other pins. The end result of all this testing is typically a set of practical PCB design recommendations, such as "keep a particular supply domain separated" or "use a bypass capacitor on this pin" or "don't route any signals near this pin".

MAINTAIN SIGNAL INTEGRITY WHEN MEASURING

As with any high speed serial test application, a number of best practices apply to ensure accurate measurement results, and you must be sure that your instrumentation offers sufficient performance and signal integrity to deliver accurate measurement results. Below are a few considerations:

Dynamic range: in general, it is best to use the full range of your oscilloscope's analog-to-digital dynamic range without clipping the amplifier. Although clipping might be acceptable when looking at a clock signal, doing this will hide ISI issues when evaluating data signals and can also affect the instrument's edge interpolation algorithm.

Sample rate: setting the oscilloscope to the highest sample rate provides the best timing resolution for the most accurate signal and jitter measurement. One exception would be if you are looking over longer time windows at lower timing accuracy.

Capture window: analyzing signals over a longer time window allows you to see low frequency modulation effects like power supply coupling and spread-spectrum clocking. Increasing the capture window unfortunately increases the analysis processing time. On SerDes systems, there is often no need to look at modulation effects below the loop bandwidth of the CDR that are tracked and rejected.

Test point access and de-embedding: ensure that you employ a mechanism for keeping the probe as close to the Tx test point as possible and as close to the Rx test point as possible. With high speed signaling test, timing, and amplitude measurements can seriously impact margin test results if the measurement process introduces unwanted signal discontinuity from long traces and/or fixturing from the actual Tx/Rx test points.

In some cases, the probe access point could be at a location where the signal is degraded due to the transmission line length. In this case, you might have to de-embed the transmission line to see what the real signal is. De-embedding involves recreating a model (using a linear method with S parameters) of the measurement channel between the instrument and the targeted test point. This model can be applied to acquired waveform data in the oscilloscope to account for those transmission line degradations (see Figure 5).

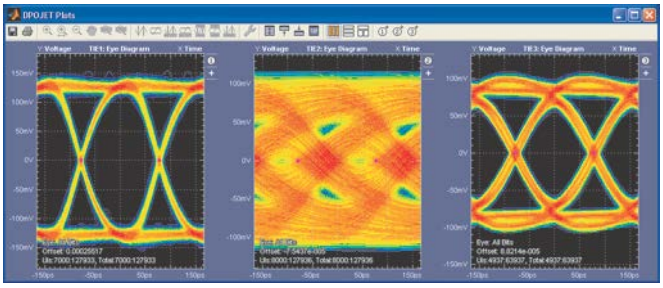

Figure 5. Eye Diagrams Illustrating Measurements Taken at Test Fixture, End of Channel, and Post-EQ

By practicing good signal integrity in your measurement techniques, you'll be better equipped to evaluate and characterize high speed technologies like JESD2024B.

SUMMARY

The recently released JESD204B interface can reliably increase data transfer bandwidth between a converter and a logic device, and a number of new devices using this interface are making their way to market. Unlike many other high speed serial interface standards, the JESD204B standard does not include an official compliance test specification, creating a number of challenges for system designers who must thoroughly test and debug their designs. Fortunately, the specification includes sufficient information to develop testing procedures, including PHY, timing, and protocol tests.

In addition to validating performance and compliance to the specification, testing can help determine the need for emphasis or equalization in a system design and help to identify unwanted sources of noise and jitter. As with any high speed serial testing effort, best practices for instrument selection, setup, and probing should be followed to ensure consistent and accurate results.

ABOUT THE AUTHORS

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Slay Your System Dragons with JESD204B

by Ian Beavers, Applications Engineer, Analog Devices, Inc.

The JESD204B serial data link interface was developed to support the growing bandwidth needs of higher speed converters. A third generation standard, it provides a higher maximum lane rate (up to 12.5 Gbps per channel) while supporting deterministic latency and harmonic frame clocking. Additionally, it now can easily move large quantities of data for processing by taking advantage of higher performance converters that are compatible and scalable with open market FPGA solutions.

FPGA providers have been talking about multigigabit serialization/deserialization (SERDES) interfaces for many years now. In the past, though, most analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) were not configured with these high speed serial interfaces. The FPGAs and the converters did not interface with any common standard that took advantage of the high SERDES bandwidth. JESD204B compliant converters can solve this problem, but this new capability introduces some questions.

What is 8b/10b encoding, and why is it needed on the JESD204B interface?

There can be no assurance of a dc balanced signal on a differential channel with random unencoded serial data, as there easily could be a larger number of either ones or zeros transmitted as opposed to the other. Random data that is sent across a serial link also has the potential to have long periods of inactivity or data that could be all ones or all zeros for a relatively long time.

When this happens, the dc balancing of an unencoded serial data stream becomes railed to one extreme or the other. At that point, when active data begins again, there is a strong potential for bit errors as the biasing of the lines is restarted. An additional long-term concern is electromigration, as a differential dc voltage is maintained on one side of the pair relative to the other. To counteract these issues, an 8b/10b encoding scheme is commonly used in differential serial data streams, including JESD204B.

In 8b/10b encoding, 10 bits are used to send the original 8 bits of information out of the source transmitter via a lookup table. This inherently accounts for a 25% inefficiency overhead (10b/8b = 1.25). In addition, the encoding allows for at least three but no more than eight bit transitions per 10-bit symbol. This ensures that there are enough transitions for the receiver to recover an embedded clock, regardless of the dynamic activity of the underlying data.

The disparity between the number of binary zeros and ones in the serial stream is kept to within ±1 using 8b/10b encoding, so the signal maintains a dc balance over time. The converse decoding of 10 bits to 8 bits must then be performed on the data stream at the receiver side to be able to recover the original data using the reverse lookup table. A more efficient 64b/66b encoding that operates on a similar principle, but with only a 3.125% overhead, is more advanced and has the potential to be used in future generations of JESD204.

The assigned JESD204B lanes of my converter do not route easily to my FPGA on my system board. There are crisscrossing pairs all over the place and it is generally susceptible to crosstalk. Is there a way to remap the assignment of the JESD204B lanes to make my layout easier?

Although converters may have JESD204B serial lanes defined by a number, letter, or other nomenclature to designate their particular relevance in the complete link, they are not required to be fixed. The specification allows for remapping of these assignments in the initial configuration data, as long as each lane and device has a unique identification. The link configuration data includes the device and lane identification numbers to identify its operation. With this information, a multiple lane transmitter could easily reassign any digital logical serial data to any physical output lane using a crossbar mux.

While it is an optional feature that the specifications allow, if an ADC vendor has a crossbar mux feature to reassign logical to physical output assignments, then the link I/O can be reconfigured in the best order for the easiest layout. The FPGA receiver can take the same initial configuration data and change the expected lane assignments to recover the data. With this ability, the routing of lanes from one device to the other can be made much easier and independent of the initial named assignment by the silicon vendor in the data sheet.

I am looking at potentially designing a converter into my system that uses a JESD204B multipoint link. How is it different from a single link?

The JESD204B specification makes provisions for what is known as a multipoint link interface. This is a communications link that connects three or more JESD204B devices. This link configuration can make sense over a single

link in some cases, depending upon how the converter is being used.

Take, for example, a dual ADC that uses JESD204B. In most cases, a dual ADC would have a single clock input to both converters. This would force simultaneous analog sampling at the same frequency. But for some unique applications, such a device could also use two separate input clocks, where each clock could drive its respective ADC independently. This would allow for a sampling phase difference between the two ADCs, or even for each ADC to be sampled with a noncoherent frequency with respect to the other. In the latter case, a single JESD204B link with data from both converters would not operate correctly without a complex back-end FIFO scheme.

A solution to this problem could be to have the dual converter use a multipoint link JESD204B interface, where each converter channel uses its own serial link output. Noncoherent clocks then could be used on each ADC, and each serial link output could easily route independently to a separate FGPA or ASIC. A multipoint link configuration can also be used when sending multiple streams of data from a single FPGA to several DACs. Device clock distribution skew can be more challenging to minimize within a multipoint configuration as the number of devices within the link grows.

What exactly is deterministic latency within JESD204B? Is this the same as the total latency of my converter?

The total latency of an ADC is the time it takes an analog sample to be clocked in, processed, and output digitally from the device. Similarly, the total latency of a DAC is the time from when the digital sample data is clocked into the part until that corresponding sample is clocked out of the analog output. Typically, these are both measured in sample clock periods of resolution, as they are frequency dependent. This is fundamentally not the same definition as the deterministic latency described by a JESD204B link implementation.

Deterministic latency across the JESD204B link is defined by the time it takes data to propagate from the parallel framed data input at the transmitter (ADC or source FPGA) to the parallel deframed data output at the receiver (DAC or receiver FPGA). This time is typically measured in either frame clock periods of resolution or device clocks (Figure 1). The definition excludes the analog front-end core of an ADC and the back-end analog core of a DAC. Not only are two devices a function in this latency computation, but so is the serial data signal routing interfacing the two. This means that the deterministic latency could be larger or smaller within a multiconverter system or multipoint link, depending upon the length of the JESD204B lane routing. Buffer delays on the receiver can help account for latency differences due to routing.

How are tail bits used in JESD204B, and what is their purpose?

The JESD204B link allows for more information space to be allotted than may actually be needed to send the converter data and control bits. If data for a particular converter or configuration does not fill up the entire space, then this "padding" is filled with what are defined as tail bits. Take, for example, a case where a space of N' = 16 is more than the parceled 13 bits of real data (N = 13 + CS = 0). Three tail bits would be used to fill the unused data space (Figure 2).

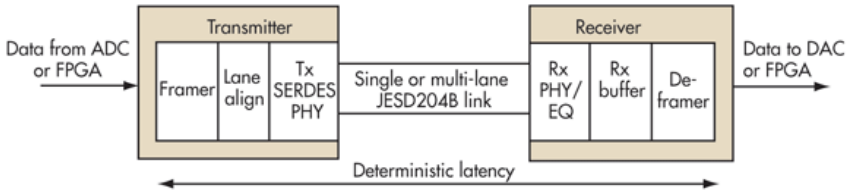

Figure 1. A Conceptual Example of JESD204B Deterministic Latency Between Framer and Deframer on Two Linked Devices. The Latency Is a Function of Three Items: the Transmitter, the Receiver, and the Interface Propagation Time Between the Two

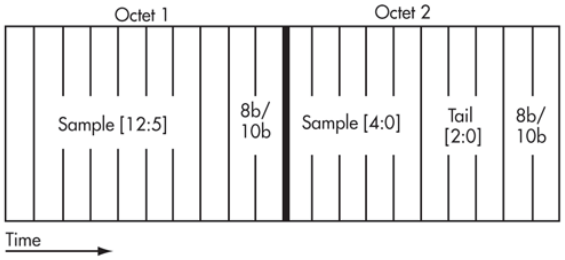

Figure 2. Three Tail Bits Can Be Used to Pad and Fill a Second Octet for N' = 16 When a Converter Only Uses 13 Bits of Sample Data

Tail bits are informationless dummy bits and are only used to completely pad the unused space. Since tail bits have the potential to cause unwanted spurious noise if they are all assigned a recurring static value, they also can be optionally represented as a pseudorandom sequence. Both the transmitter and receiver must understand that these bits are informationless based on the link configuration. The receiver can therefore simply discard them from the stream of relevant data.

My link patterns work fine, but I am not getting converter data transmitted in a normal operating mode. In past generations of converters, low voltage differential signaling (LVDS) and parallel interfaces allowed easy probing/debugging of a least significant bit (LSB) or most significant bit (MSB) pin of a DAC or ADC to see if the functional converter operation was taking place. How can I probe an MSB or LSB when using the JESD204B interface?

This is one of the few drawbacks to the JESD204B interface. It is not easy to electrically probe an LSB or MSB I/O to see if there is correct activity to and from the converter. This is because the sample data is serialized per channel, so a particular weighted bit cannot easily be probed electrically. However, a few options can be used to debug a system issue when you quickly want to know what, if any, valid data is being sent or received from your converter.

Some oscilloscope vendors provide real-time data processing to serially decode 8b/10b data and display an unencoded stream on the oscilloscope screen. Unscrambled data can be probed in this fashion to determine what activity is taking place on the link.

FPGA vendors offer an internal probing software tool that gives system designers a method to observe the I/O data sent and received from within the FPGA by connecting it via a USB dongle to a computer. Also, some ASICs and converters offer an internal serial loop-back self-test mode that can be used to help decipher data issues on the link.

How do I calculate the lane rate for my converter, given that I know the other parameters of the link?

System designers using JESD204B can easily compute the number of lanes or lane rate for their link given that they know the other key criteria of their converter, ASIC, or FPGA. There is a mathematical relationship for all of the basic link parameters below such that one unknown variable can be computed and solved. Based on the result, system designers can choose other parameters to change the link operation within the confines of the converter or FPGA architecture:

$$\textit{Lane rate} = (M \times N' \times [10/8] \times Fs)/L$$

where:

M is the number of converters on the link.

N' is the number of informational bits sent in a sample (including sample resolution, control and tail bits).

Fs is the device or sample clock.

L is the lane count.

Lane rate is the bit rate for a single lane.

10/8 is the link overhead due to 8b/10b encoding.

For example, consider a dual ADC with N' = 16, Fs = 235 MHz, using two lanes. What is the lane rate?

$$\textit{Lane rate} = [2 \times 16 \times 1.25 \times 235 \text{ MHz}]/2$$

$$\textit{Lane rate} = 4700 \text{ Mbps or } 4.7 \text{ Gbps}$$

What is an application layer, and what does it do?

An application layer is a method provided for in JESD204B that allows sample data to be mapped outside the normal specification. This can be useful for certain converter modes that need to pass data samples in sizes that are relatively different from the N' of the link.

An otherwise inefficient arrangement on the link can be made more efficient with a lower lane count or lower lane speed by using an application layer. Both the transmitter and receiver need to be configured to understand a specific application layer, as it can be custom or uniquely designed by a particular converter mode. Figure 3 shows an example where five samples are partitioned into a space typically occupied by only four.

When using the equation from the previous question for application layer calculations, the effective N', instead of the actual N', needs to be used. For example, in the application layer case shown below, although the actual JESD024B sample N' is 16, the effective N' for ADC samples can be figured since 64 bits are used to send five samples. Therefore, Neff = 64/5 = 12.8. With all other variables held equal, the lane rate could then be run 20% slower:

$$Neff/N' = 12.8/16 = 0.8.$$

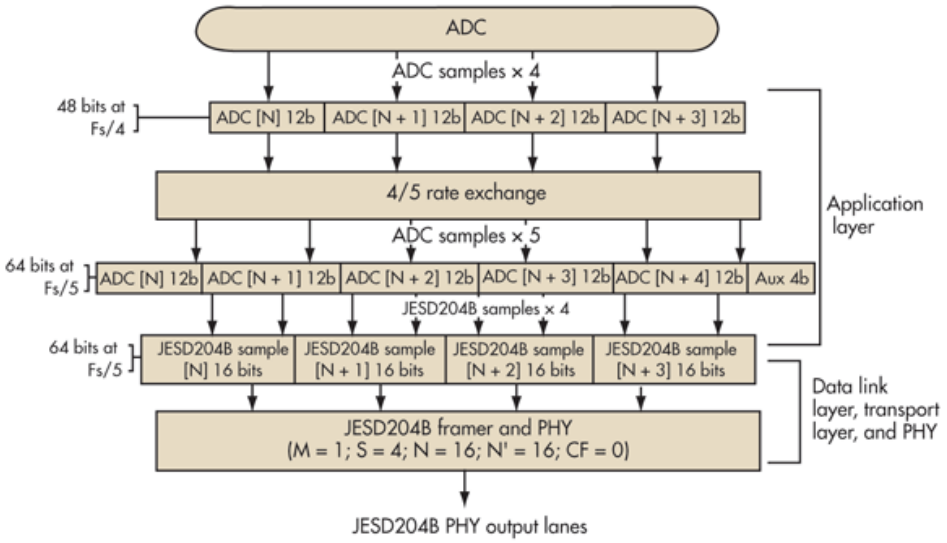

Figure 3. An ADC Application Layer Can ReMap Five 12-Bit ADC Samples into the Space Used by Four JESD204B N' = 16 Samples. Four Bits of Extra Auxiliary Information Can Be Made Available for Additional Use

What's next?

As JESD204B continues to proliferate within the data converter market, intellectual property (IP) capabilities on FPGA platforms should help speed its adoption. Future discussions on the subject should only grow, albeit with additional complexity, as more engineers become involved and start designing new systems.

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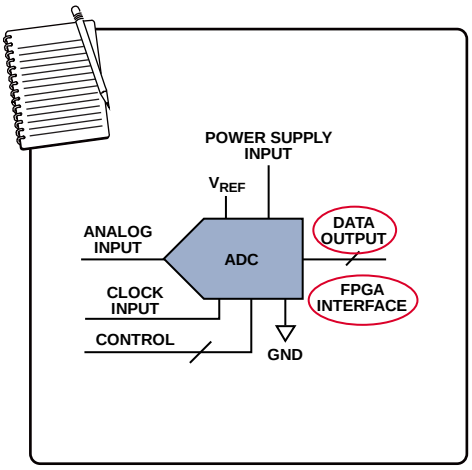
Interfacing FPGAs to an ADC Converter's Digital Data Output

by the Applications Engineering Group, Analog Devices, Inc.



The Applications Engineering Notebook Educational Series

IN THIS NOTEBOOK

Interfacing field programmable gate arrays (FPGAs) to analog-to-digital converter (ADC) output is a common engineering challenge. This notebook includes an overview of various interface protocols and standards as well as application tips and techniques for utilizing LVDS in high speed data converter implementations.

TABLE OF CONTENTS

REVISION HISTORY

1/13—Rev. 0 to Rev. A

Deleted Using Adapter Boards Section 11

1/12—Revision 0: Initial Version

INTERFACE STYLES AND STANDARDS

Interfacing field programmable gate arrays (FPGAs) to analog-to-digital converter (ADC) digital data output is a common engineering challenge. The task is complicated by the fact that ADCs use a variety of digital data styles and standards. Single data rate (SDR) CMOS is very common for lower speed data interfaces, typically under 200 MHz. In this case, data is transitioned on one edge of the clock by the transmitter and received by the receiver on the other clock edge. This ensures the data has plenty of time to settle before being sampled by the receiver. In double data rate (DDR) CMOS, the transmitter transitions data on every clock edge. This allows for twice as much data to be transferred in the same amount of time as SDR; however, the timing for proper sampling by the receiver is more complicated.

Parallel low voltage differential signaling (LVDS) is a common standard for high speed data converters. It uses differential signaling with a P and N wire for each bit to achieve speeds up to the range of 1.6 Gbps with DDR or 800 MHz in the latest FPGAs. Parallel LVDS consumes less power than CMOS, but requires twice the number of wires, which can make routing difficult. Though not part of the LVDS standard, LVDS is commonly used in data converters with a "source synchronous" clocking system. In this setup, a clock, which is in-phase with the data, is transmitted alongside the data. The receiver can then use this clock to capture the data easier, since it now knows the data transitions.

FPGA logic is often not fast enough to keep up with the bus speed of high speed converters, so most FPGAs have serializer/deserializer (SERDES) blocks to convert a fast, narrow serial interface on the converter side to a wide, slow parallel interface on the FPGA side. For each data bit in the bus, this block outputs 2, 4, or 8 bits, but at ½, ¼, or 1/8 the clock rate, effectively deserializing the data. The data is processed by wide busses inside the FPGA that run at much slower speeds than the narrow bus going to the converter.

The LVDS signaling standard is also used in serial links, mostly on high speed ADCs. Serial LVDS is typically used when pin count is more important than interface speed. Two clocks, the data rate clock and the frame clock, are often used. All the considerations mentioned in the parallel LVDS section also apply to serial LVDS. Parallel LVDS simply consists of multiple serial LVDS lines.

I^2C uses two wires: clock and data. It supports a large number of devices on the bus without additional pins. I^2C is relatively slow, 400 kHz to 1 MHz with protocol overhead. It is commonly used on slow devices where part size is a concern. I^2C is also often used as a control interface or data interface.

SPI uses 3 or 4 wires:

- Clock
- Data in and data out (4-wire), or bidirectional data in/data out (3-wire)
- Chip select (one per nonmaster device)

SPI supports as many devices as the number of available chip select lines. It provides speeds up to about 100 MHz and is commonly used as both a control interface and data interface.

Serial PORT (SPORT), a CMOS-based bidirectional interface, uses one or two data pins per direction. Its adjustable word length provides better efficiency for non %8 resolutions. SPORT offers time domain multiplexing (TDM) support and is commonly used on audio/media converters and high channel count converters. It offers performance of about 100 MHz per pin. SPORT is supported on Blackfin processors and offers straightforward implementation on FPGAs. SPORT is generally used for data only, although control characters can be inserted.

JESD204 is a JEDEC standard for high speed serial links between a single host, such as an FPGA or ASIC, and one or more data converters. The latest spec provides up to 3.125 Gbps per lane or differential pair. Future revisions may specify 6.25 Gbps and above. The lanes use 8B/10B encoding, reducing effective bandwidth of the lane to 80% of the theoretical value. The clock is embedded in data stream so there are no extra clock signals. Multiple lanes can be bonded together to increase throughput while the data link layer protocol ensures data integrity. JESD204 requires significantly more resources in FPGA/ASIC for data framing than simple LVDS or CMOS. It dramatically reduces wiring requirements at the expense of a more expensive FPGA and more sophisticated PCB routing.

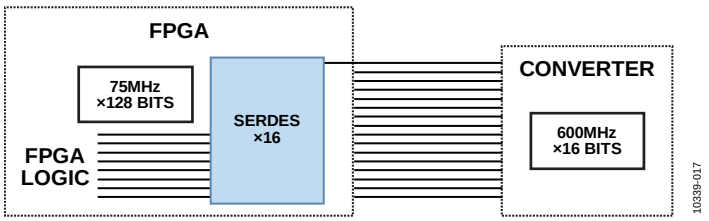


Figure 1. SERDES Blocks in FPGA Interface with High Speed Serial Interfaces on Converter

GENERAL RECOMMENDATIONS

Some general recommendations are helpful in interfacing between ADCs and FPGAs.

- Use external resistor terminations at the receiver, FPGA, or ASIC, rather than the internal FPGA terminations, to avoid reflections due to mismatch that can break the timing budget.
- Don't use one DCO from one ADC if you are using multiple ADCs in the system.
- Don't use a lot of "tromboning" when laying out digital traces to the receiver to keep all traces equal length.
- Use series terminations on CMOS outputs to slow edge rates down and limit switching noise. Verify that the right data format (twos complement, offset binary) is being used.

With single-ended CMOS digital signals, logic levels move at about 1 V/nS, typical output loading is 10 pF maximum, and typical charging currents are 10 mA/bit. Charging current should be minimized by using the smallest capacitive load possible. This can usually be accomplished by driving only one gate with the shortest trace possible, preferably without any vias. Charging current can also be minimized by using a damping resistor in digital outputs and inputs.

The time constant of the damping resistor and the capacitive load should be approximately 10% of the period of the sample rate. If the clock rate is 100 MHz and the loading is 10 pF, then the time constant should be 10% of 10 nS or 1 nS. In this case, R should be 100 Ω. For optimal signal-to-noise ratio (SNR) performance, a 1.8 V DRVDD is preferred over 3.3 V DRVDD. However, SNR is degraded when driving large capacitive loads. CMOS outputs are useable up to about 200 MHz sampling clocks. If driving two output loads or trace length is longer than 1 or 2 inches, a buffer is recommended.

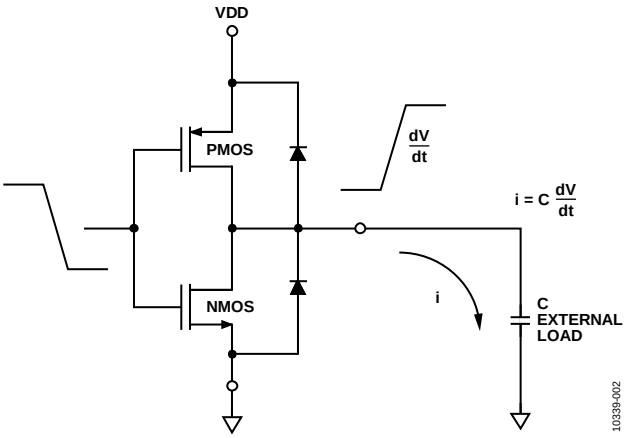


Figure 2. Typical CMOS Digital Output Drivers

ADC digital outputs should be treated with care because transient currents can increase the noise and distortion of the ADC by coupling back into the analog input.

Typical CMOS drivers shown in Figure 2 are capable of generating large transient currents, especially when driving capacitive loads. Particular care must be taken with CMOS data output ADCs so that these currents are minimized and do not generate additional noise and distortion in the ADC.

TYPICAL EXAMPLES

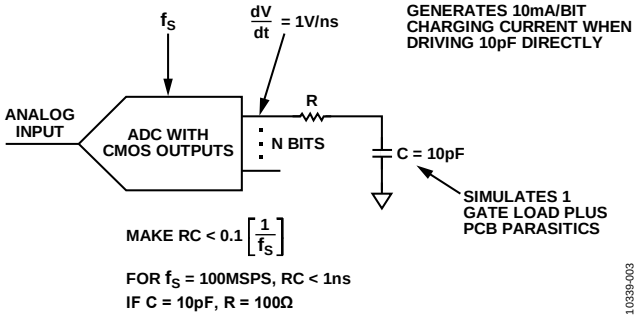


Figure 3. Use Series Resistance to Minimize Charging Current of CMOS Digital Outputs

Figure 3 shows the case of a 16-bit parallel CMOS output ADC. With a 10 pF load on each output, simulating one gate load plus PCB parasitics, each driver generates a charging current of 10 mA when driving a 10 pF load.

The total transient current for the 16-bit ADC can, therefore, be as high as 16 × 10 mA = 160 mA. These transient currents can be suppressed by adding a small resistor, R, in series with each data output. The value of the resistor should be chosen so that the RC time constant is less than 10% of the total sampling period. For *f*s = 100 MSPS, RC should be less than 1 ns. With C = 10 pF, an R of about 100 Ω is optimum. Choosing larger values of R can degrade output data settling time and interfere with proper data capture. Capacitive loading on CMOS ADC outputs should be limited to a single gate load, usually an external data capture register. Under no circumstances should the data output be connected directly to a noisy data bus. An intermediate buffer register must be used to minimize direct loading of the ADC outputs.

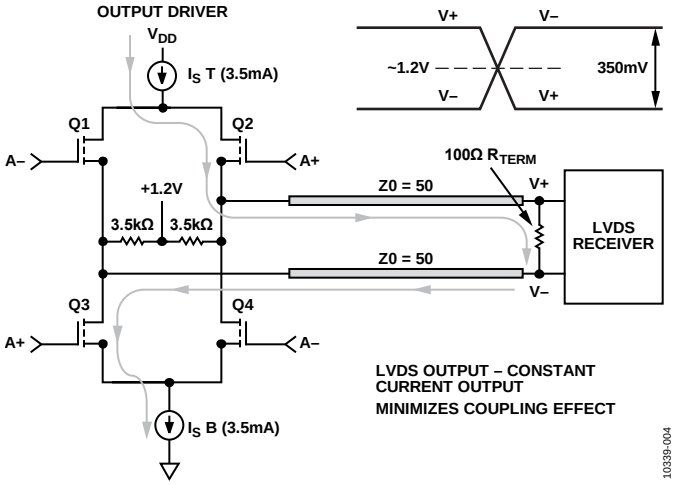


Figure 4. Typical LVDS Driver Design

Figure 4 shows a standard LVDS driver in CMOS. The nominal current is 3.5 mA and the common-mode voltage is 1.2 V. The swing on each input at the receiver is therefore 350 mV p-p when driving a 100 Ω differential termination resistor. This corresponds to a differential swing of 700 mV p-p. These figures are derived from the LVDS specification.

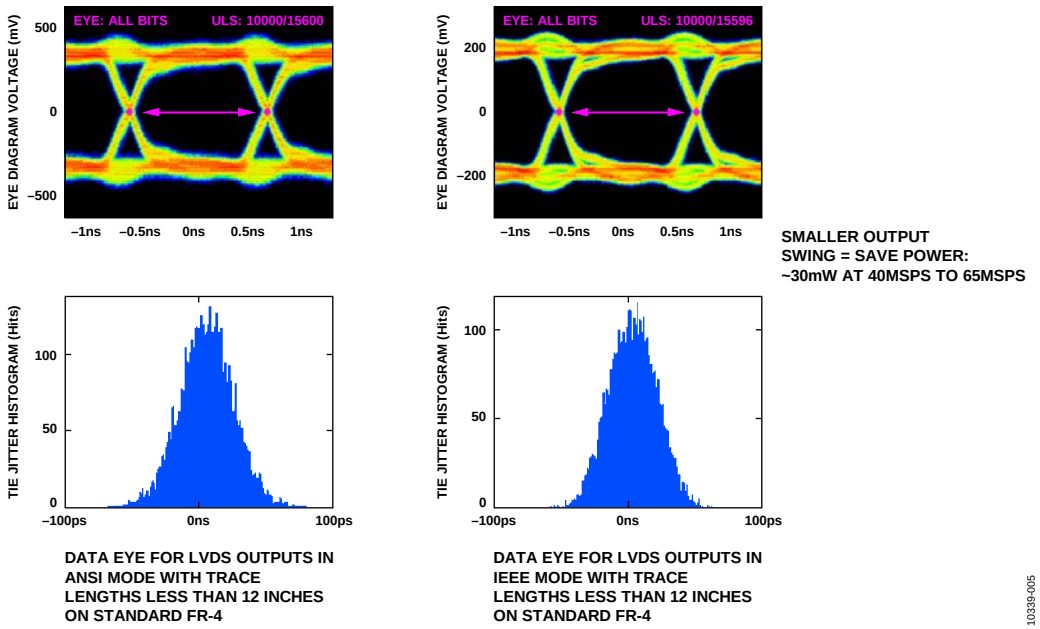


Figure 5. ANSI vs. IEEE LVDS Standards

There are two LVDS standards: one is defined by ANSI and the other by IEEE. While the two standards are similar and generally compatible with each other, they are not identical. Figure 5 compares an eye diagram and jitter histogram for each of the two standards. IEEE standard LVDS has a reduced swing of 200 mV p-p as compared to the ANSI standard of 320 mV p-p. This helps to save power on the digital outputs. For this reason, use the IEEE standard if it will accommodate the application and connections that need to be made to the receiver.

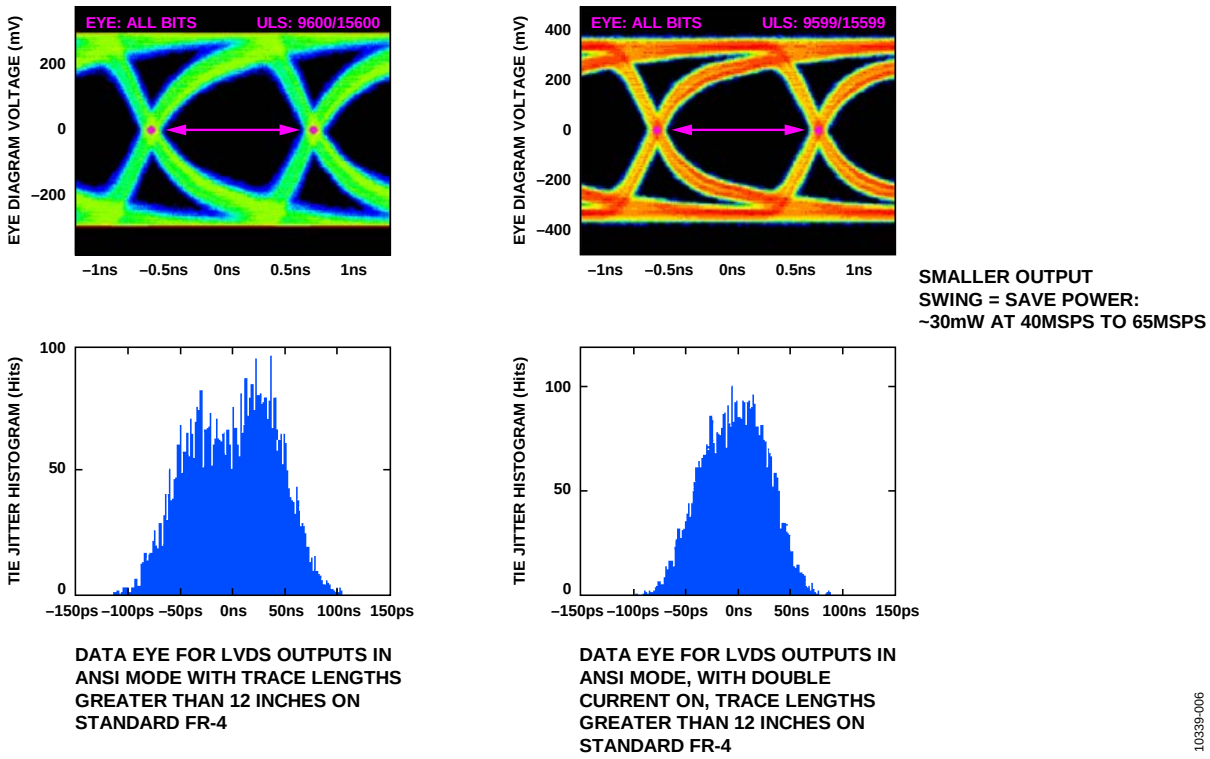


Figure 6. ANSI vs. IEEE LVDS Standards with Traces over 12 Inches

Figure 6 compares the ANSI and IEEE LVDS standards with long trace lengths above 12 inches or 30 cm. Both graphs are driven at the ANSI version standard. In the graph on the right, the output current is doubled. Doubling the output current cleans up the eye and improves the jitter histogram.

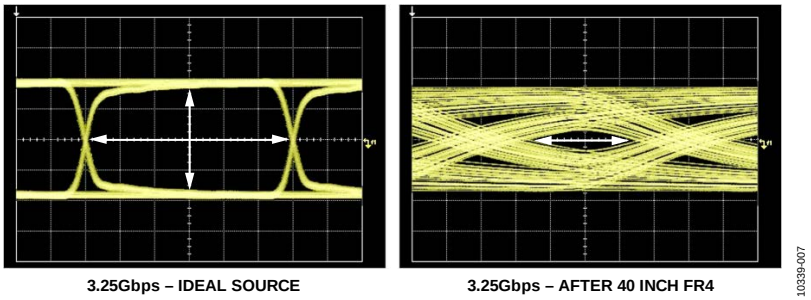


Figure 7. Effects of FR4 Channel Loss

Note the effects of a long trace on FR4 material in Figure 7. The left plot shows an ideal eye diagram, right at the transmitter. At the receiver, 40 inches away, the eye has almost closed and the receiver has difficulty recovering the data.

TROUBLESHOOTING TIPS

ADC WITH MISSING BIT 14

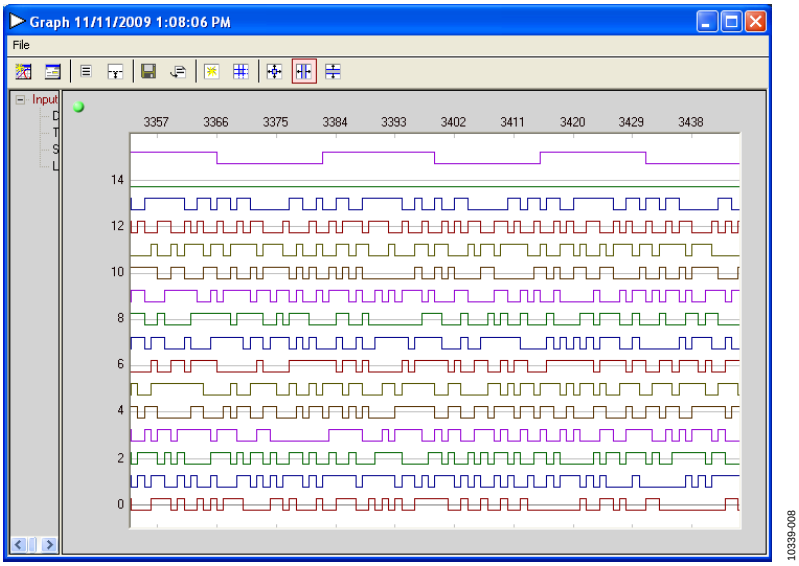


Figure 8. AD9268 ADC with Missing Bit 14

In Figure 8, a VisualAnalog digital display of the data bits shows that Bit 14 never toggles. This could indicate an issue with the part, the PCB, the receiver, or, that the unsigned data simply is not large enough to toggle the most significant bit.

ADC FREQUENCY DOMAIN PLOT WITH MISSING BIT 14

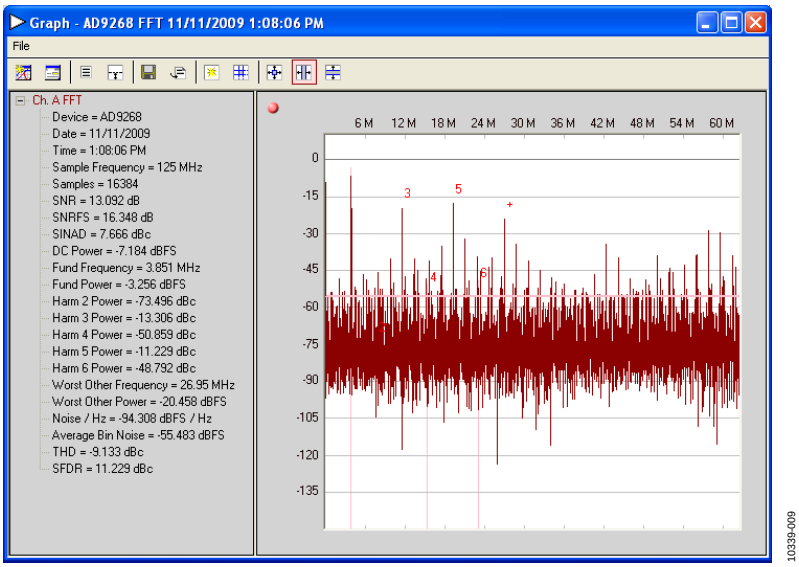


Figure 9. AD9268 ADC Frequency Domain Plot with Missing Bit 14

Figure 9 shows a frequency domain view of the previous digital data where Bit 14 is not toggling. The plot shows that the bit is significant and there is an error somewhere in the system.

ADC TIME DOMAIN PLOT WITH MISSING BIT 14

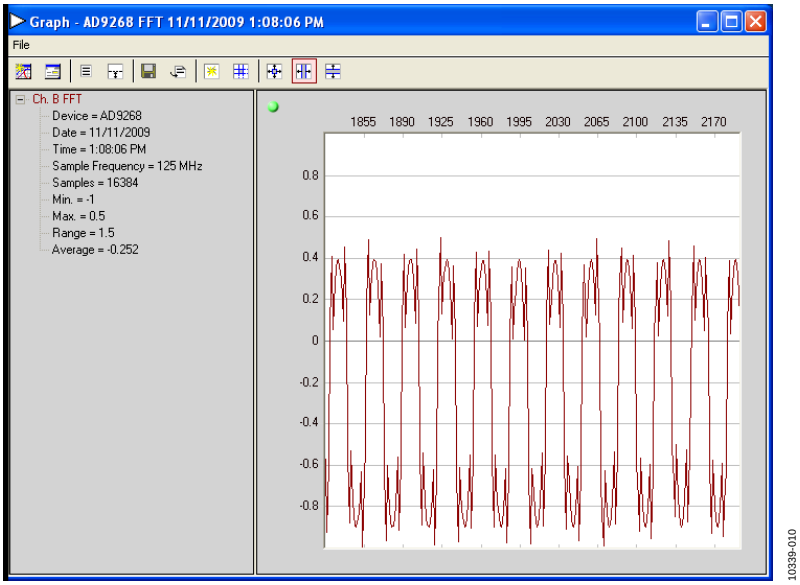


Figure 10. AD9268 ADC Time Domain Plot with Missing Bit 14

Figure 10 is a time domain plot of the same data. Instead of a smooth sine wave, the data is offset and has significant peaks at points throughout the waveform.

ADC WITH BIT 9 AND BIT 10 SHORTED TOGETHER

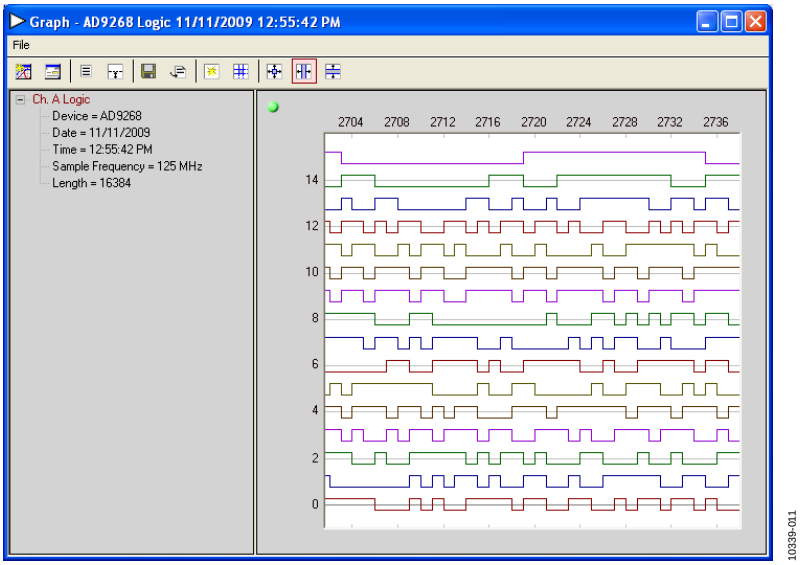


Figure 11. AD9268 ADC with Bit 9 and Bit 10 Shorted Together

In Figure 11, instead of missing a bit, two bits are shorted together so that the receiver always sees the same data on the two pins.

ADC FREQUENCY DOMAIN PLOT WITH BIT 9 AND BIT 10 SHORTED TOGETHER

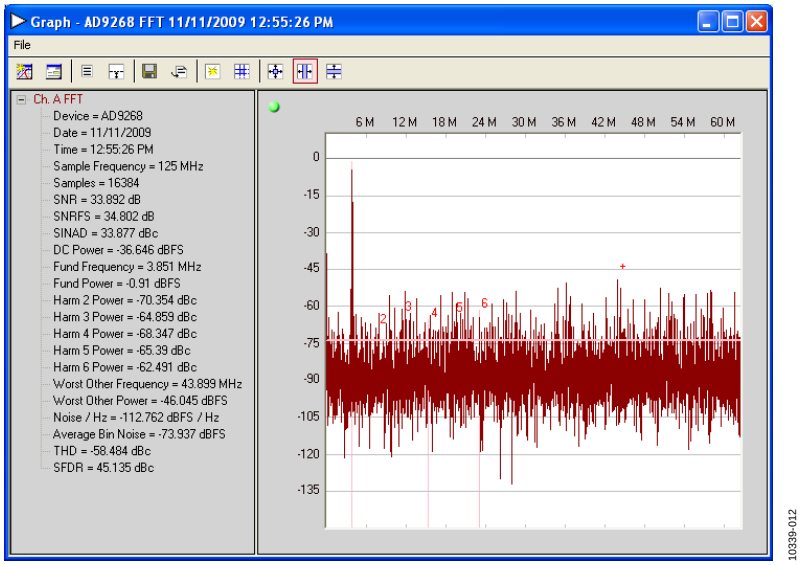


Figure 12. AD9268 ADC Frequency Domain Plot with Bit 9 and Bit 10 Shorted Together

Figure 12 shows a frequency domain view of the same case where two bits are shorted together. While the fundamental tone is clearly present, the noise floor is significantly worse than it should be. The degree to which the floor is distorted depends on which bits are shorted.

ADC TIME DOMAIN PLOT WITH BIT 9 AND BIT 10 SHORTED TOGETHER

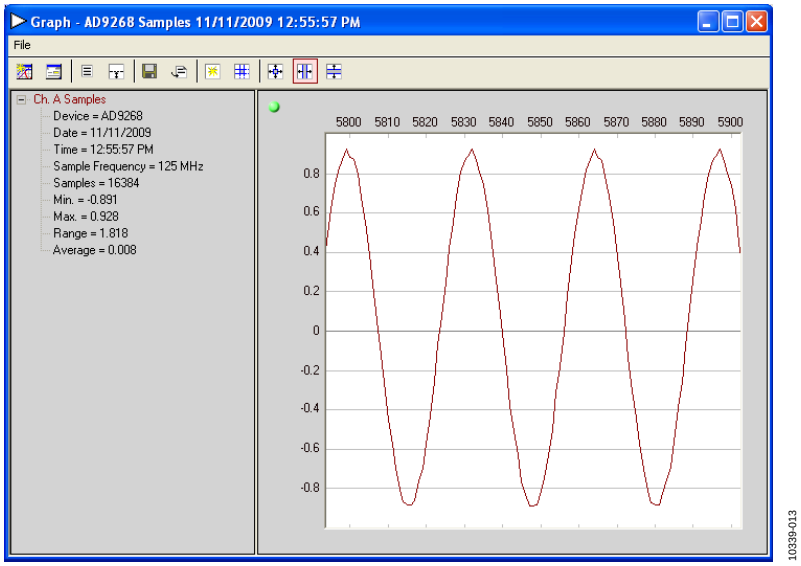


Figure 13. AD9268 ADC Time Domain Plot with Bit 9 and Bit 10 Shorted Together

In this time-domain view shown in Figure 13, the issue is less obvious. Although some smoothness is lost in the peaks and valleys of the wave, this is also common when the sample rate is close to the waveform's frequency.

TIME DOMAIN PLOT WITH INVALID DATA AND CLOCK TIMING

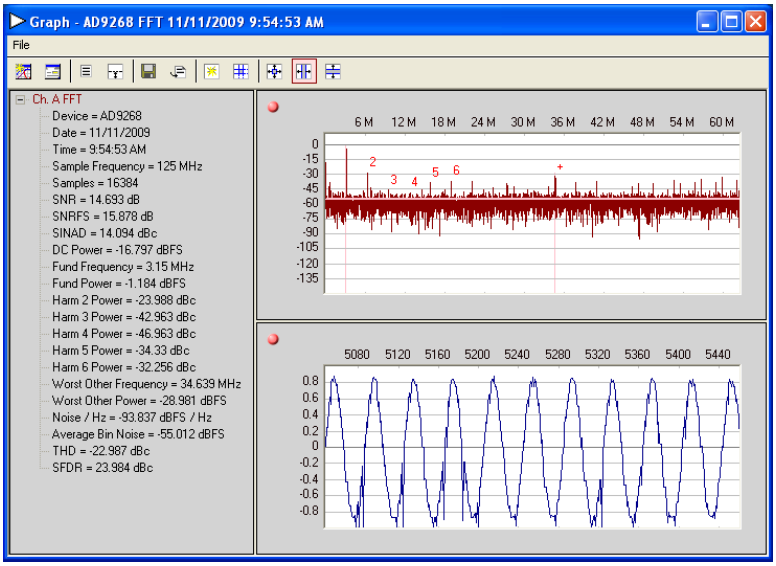


Figure 14. AD9268 Time Domain Plot with Invalid Data and Clock Timing

Figure 14 shows a converter with invalid timing, in this case caused by setup/hold problems. Unlike the previous errors, which generally showed themselves during each cycle of the data, timing errors are usually less consistent. Less severe timing errors may be intermittent. These plots show the time domain and frequency domain of a data capture that is not meeting timing. Notice that the errors in the time domain are not consistent between cycles. Also, note the elevated noise floor in the FFT/frequency domain. This usually indicates a missing bit, which can be caused by incorrect time alignment.

ZOOMED-IN TIME DOMAIN PLOT WITH INVALID DATA AND CLOCK TIMING

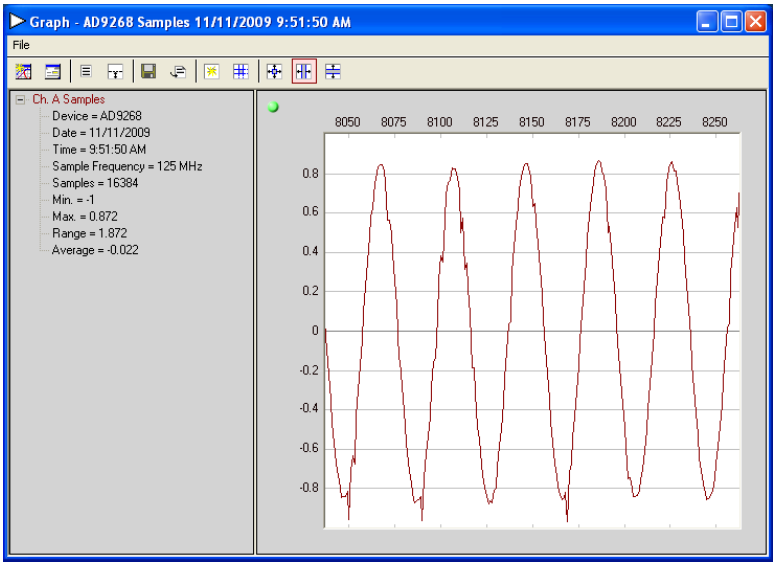


Figure 15. AD9268 Zoom-In Time Domain Plot with Invalid Data and Clock Timing

Figure 15 is a closer view of the time domain timing error shown in the Figure 14. Again, note that the errors are not consistent from cycle to cycle, but that certain errors do repeat. An example is the negative spike on the valley of several cycles in this plot.

Page 11 of 12 and Page 12 of 12 are blank.

14-Bit, 170 MSPS/250 MSPS, JESD204B, Dual Analog-to-Digital Converter

Data Sheet **AD9250**

FEATURES

- JESD204B Subclass 0 or Subclass 1 coded serial digital outputs
- Signal-to-noise ratio (SNR) = 70.6 dBFS at 185 MHz AIN and 250 MSPS
- Spurious-free dynamic range (SFDR) = 88 dBc at 185 MHz AIN and 250 MSPS
- Total power consumption: 711 mW at 250 MSPS
- 1.8 V supply voltages
- Integer 1-to-8 input clock divider
- Sample rates of up to 250 MSPS
- IF sampling frequencies of up to 400 MHz
- Internal analog-to-digital converter (ADC) voltage reference
- Flexible analog input range
  - 1.4 V p-p to 2.0 V p-p (1.75 V p-p nominal)
- ADC clock duty cycle stabilizer (DCS)
- 95 dB channel isolation/crosstalk
- Serial port control
- Energy saving power-down modes
- User-configurable, built-in self-test (BIST) capability

APPLICATIONS

- Diversity radio systems
- Multimode digital receivers (3G)
  - TD-SCDMA, WiMAX, WCDMA, CDMA2000, GSM, EDGE, LTE
- DOCSIS 3.0 CMTS upstream receive paths
- HFC digital reverse path receivers
- I/Q demodulation systems
- Smart antenna systems
- Electronic test and measurement equipment
- Radar receivers
- COMSEC radio architectures
- IED detection/jamming systems
- General-purpose software radios
- Broadband data applications

FUNCTIONAL BLOCK DIAGRAM

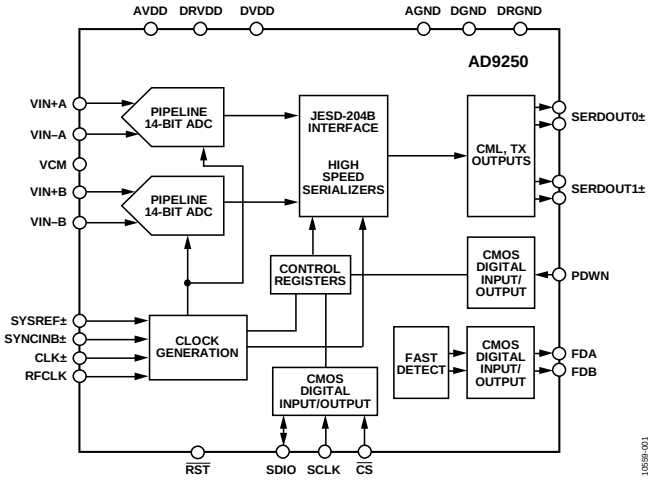


Figure 1.

PRODUCT HIGHLIGHTS

1. Integrated dual, 14-bit, 170 MSPS/250 MSPS ADC.
2. The configurable JESD204B output block supports up to 5 Gbps per lane.
3. An on-chip, phase-locked loop (PLL) allows users to provide a single ADC sampling clock; the PLL multiplies the ADC sampling clock to produce the corresponding JESD204B data rate clock.
4. Support for an optional RF clock input to ease system board design.
5. Proprietary differential input maintains excellent SNR performance for input frequencies of up to 400 MHz.
6. Operation from a single 1.8 V power supply.
7. Standard serial port interface (SPI) that supports various product features and functions such as controlling the clock DCS, power-down, test modes, voltage reference mode, over range fast detection, and serial output configuration.

Rev. A Document Feedback

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TABLE OF CONTENTS

REVISION HISTORY

3/13—Rev. 0 to Rev. A

Changes to High Level Input Current and Low Level Input Current; Table 3 ... 6
Changes to Table 4 ... 8
Changes to Figure 3 Caption ... 9
Changes to Digital Inputs Description; Table 8 ... 11
Changes to JESD204B Synchronization Details Section ... 24
Changes to Configure Detailed Options Section ... 25
Changes to Fast Threshold Detection (FDA and FDB) Section ... 30
Deleted Built-In Self-Test (BIST) and Output Test Section ... 32
Changes to Transfer Register Map Section ... 34
Changes to Table 17 ... 35

10/12—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9250 is a dual, 14-bit ADC with sampling speeds of up to 250 MSPS. The AD9250 is designed to support communications applications where low cost, small size, wide bandwidth, and versatility are desired.

The ADC cores feature a multistage, differential pipelined architecture with integrated output error correction logic. The ADC cores feature wide bandwidth inputs supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. A duty cycle stabilizer is provided to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance. The JESD204B high speed serial interface reduces board routing requirements and lowers pin count requirements for the receiving device.

By default, the ADC output data is routed directly to the two JESD204B serial output lanes. These outputs are at CML voltage levels. Four modes support any combination of M = 1 or 2 (single or dual converters) and L = 1 or 2 (one or two lanes). For dual ADC mode, data can be sent through two lanes at the maximum sampling rate of 250 MSPS. However, if data is sent through one lane, a sampling rate of up to 125 MSPS is supported. Synchronization inputs (SYNCINB± and SYSREF±) are provided.

Flexible power-down options allow significant power savings, when desired. Programmable overrange level detection is supported for each channel via the dedicated fast detect pins.

Programming for setup and control are accomplished using a 3-wire SPI-compatible serial interface.

The AD9250 is available in a 48-lead LFCSP and is specified over the industrial temperature range of −40°C to +85°C. This product is protected by a U.S. patent.

SPECIFICATIONS

ADC DC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, DVDD = 1.8 V, maximum sample rate for speed grade, VIN = −1.0 dBFS differential input, 1.75 V p-p full-scale input range, duty cycle stabilizer (DCS) enabled, link parameters used were M = 2 and L = 2, unless otherwise noted.

Table 1.

		AD9250-170			AD9250-250			
Parameter	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	14			14			Bits
ACCURACY								
No Missing Codes	Full		Guaranteed			Guaranteed		
Offset Error	Full	−16		+16	−16		+16	mV
Gain Error	Full	−6		+2	−6		+2.5	%FSR
Differential Nonlinearity (DNL)	Full			±0.75			±0.75	LSB
	25°C		±0.25			±0.25		LSB
Integral Nonlinearity (INL)[1]	Full			±2.1			±3.5	LSB
	25°C		±1.5			±1.5		LSB
MATCHING CHARACTERISTIC								
Offset Error	Full	−15		+15	−15		+15	mV
Gain Error	Full	−2		+3.5	−2		+3	%FSR
TEMPERATURE DRIFT								
Offset Error	Full		±2			±2		ppm/°C
Gain Error	Full		±16			±44		ppm/°C
INPUT REFERRED NOISE								
VREF = 1.0 V	25°C		1.49			1.49		LSB rms
ANALOG INPUT								
Input Span	Full		1.75			1.75		V p-p
Input Capacitance[2]	Full		2.5			2.5		pF
Input Resistance[3]	Full		20			20		kΩ
Input Common-Mode Voltage	Full		0.9			0.9		V
POWER SUPPLIES								
Supply Voltage								
AVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
Supply Current								
I_{AVDD}	Full		233	260		255	280	mA
$I_{DRVDD} + I_{DVDD}$	Full		104	113		140	160	mA
POWER CONSUMPTION								
Sine Wave Input	Full		607			711		mW
Standby Power[4]	Full		280			339		mW
Power-Down Power	Full		9			9		mW

[1] Measured with a low input frequency, full-scale sine wave.
[2] Input capacitance refers to the effective capacitance between one differential input pin and its complement.
[3] Input resistance refers to the effective resistance between one differential input pin and its complement.
[4] Standby power is measured with a dc input and the CLK± pin active.

ADC AC SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, DVDD = 1.8 V, maximum sample rate for speed grade, VIN = −1.0 dBFS differential input, 1.75 V p-p full-scale input range, link parameters used were M = 2 and L = 2, unless otherwise noted.

Table 2.

		AD9250-170			AD9250-250			
Parameter[1]	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE-RATIO (SNR)								
f_{IN} = 30 MHz	25°C		72.5			72.1		dBFS
f_{IN} = 90 MHz	25°C		72.0			71.7		dBFS
	Full	70.7						dBFS
f_{IN} = 140 MHz	25°C		71.4			71.2		dBFS
f_{IN} = 185 MHz	25°C		70.7			70.6		dBFS
	Full				69.3			dBFS
f_{IN} = 220 MHz	25°C		70.1			70.0		dBFS
SIGNAL-TO-NOISE AND DISTORTION (SINAD)								
f_{IN} = 30 MHz	25°C		71.3			70.7		dBFS
f_{IN} = 90 MHz	25°C		70.9			70.5		dBFS
	Full	69.6						dBFS
f_{IN} = 140 MHz	25°C		70.3			70.0		dBFS
f_{IN} = 185 MHz	25°C		69.6			69.5		dBFS
	Full				68.0			dBFS
f_{IN} = 220 MHz	25°C		68.9			68.8		dBFS
EFFECTIVE NUMBER OF BITS (ENOB)								
f_{IN} = 30 MHz	25°C		11.5			11.5		Bits
f_{IN} = 90 MHz	25°C		11.4			11.4		Bits
f_{IN} = 140 MHz	25°C		11.3			11.3		Bits
f_{IN} = 185 MHz	25°C		11.1			11.2		Bits
f_{IN} = 220 MHz	25°C		10.9			11.0		Bits
SPURIOUS-FREE DYNAMIC RANGE (SFDR)								
f_{IN} = 30 MHz	25°C		92			89		dBc
f_{IN} = 90 MHz	25°C		95			86		dBc
	Full	78						dBc
f_{IN} = 140 MHz	25°C		91			86		dBc
f_{IN} = 185 MHz	25°C		86			88		dBc
	Full				80			dBc
f_{IN} = 220 MHz	25°C		85			88		dBc
WORST SECOND OR THIRD HARMONIC								
f_{IN} = 30 MHz	25°C		−92			−89		dBc
f_{IN} = 90 MHz	25°C		−95			−87		dBc
	Full			−78				dBc
f_{IN} = 140 MHz	25°C		−91			−86		dBc
f_{IN} = 185 MHz	25°C		−86			−88		dBc
	Full						−80	dBc
f_{IN} = 220 MHz	25°C		−85			−88		dBc
WORST OTHER (HARMONIC OR SPUR)								
f_{IN} = 30 MHz	25°C		−95			−94		dBc
f_{IN} = 90 MHz	25°C		−94			−96		dBc
	Full			−78				dBc
f_{IN} = 140 MHz	25°C		−97			−96		dBc
f_{IN} = 185 MHz	25°C		−96			−88		dBc
	Full						−80	dBc
f_{IN} = 220 MHz	25°C		−93			−91		dBc

Parameter[1]	Temperature	AD9250-170 Min	AD9250-170 Typ	AD9250-170 Max	AD9250-250 Min	AD9250-250 Typ	AD9250-250 Max	Unit
TWO-TONE SFDR								
f_{IN} = 184.12 MHz (−7 dBFS), 187.12 MHz (−7 dBFS)	25°C		87			84		dBc
CROSSTALK[2]	Full		95			95		dB
FULL POWER BANDWIDTH[3]	25°C		1000			1000		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] Crosstalk is measured at 100 MHz with −1.0 dBFS on one channel and no input on the alternate channel.
[3] Full power bandwidth is the bandwidth of operation determined by where the spectral power of the fundamental frequency is reduced by 3 dB.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DRVDD = 1.8 V, DVDD = 1.8 V, maximum sample rate for speed grade, VIN = −1.0 dBFS differential input, 1.75 V p-p full-scale input range, DCS enabled, link parameters used were M = 2 and L = 2, unless otherwise noted.

Table 3.

Parameter	Temperature	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK−)					
Input CLK± Clock Rate	Full	40		625	MHz
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND		AVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	0		+60	µA
Low Level Input Current	Full	−60		0	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
RF CLOCK INPUT (RFCLK)					
Input CLK± Clock Rate	Full	650		1500	MHz
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Bias	Full		0.9		V
Input Voltage Range	Full	AGND		AVDD	V
Input Voltage Level					
High	Full	1.2		AVDD	V
Low	Full	AGND		0.6	V
High Level Input Current	Full	0		+150	µA
Low Level Input Current	Full	−150		0	µA
Input Capacitance	Full		1		pF
Input Resistance (AC-Coupled)	Full	8	10	12	kΩ
SYNCIN INPUT (SYNCINB+/SYNCINB−)					
Logic Compliance			LVDS		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage Range	Full	0.3		3.6	V p-p
Input Voltage Range	Full	DGND		DVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	−5		+5	µA
Low Level Input Current	Full	−5		+5	µA
Input Capacitance	Full		1		pF
Input Resistance	Full	12	16	20	kΩ

Parameter	Temperature	Min	Typ	Max	Unit
SYSREF INPUT (SYSREF±)					
Logic Compliance			LVDS		
Internal Common-Mode Bias	Full		0.9		V
Differential Input Voltage Range	Full	0.3		3.6	V p-p
Input Voltage Range	Full	AGND		AVDD	V
Input Common-Mode Range	Full	0.9		1.4	V
High Level Input Current	Full	−5		+5	µA
Low Level Input Current	Full	−5		+5	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
LOGIC INPUT ($\overline{RST}$, $\overline{CS}$)[1]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−5		+5	µA
Low Level Input Current	Full	−100		−45	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (SCLK/PDWN)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	45		100	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUTS (SDIO)[2]					
High Level Input Voltage	Full	1.22		2.1	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	45		100	µA
Low Level Input Current	Full	−10		10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
DIGITAL OUTPUTS (SERDOUT0±/SERDOUT1±)					
Logic Compliance	Full		CML		
Differential Output Voltage (V_{OD})	Full	400	600	750	mV
Output Offset Voltage (V_{OS})	Full	0.75	DRVDD/2	1.05	V
DIGITAL OUTPUTS (SDIO/FDA/FDB)					
High Level Output Voltage (V_{OH})	Full				
I_{OH} = 50 µA	Full	1.79			V
I_{OH} = 0.5 mA	Full	1.75			V
Low Level Output Voltage (V_{OL})	Full				
I_{OL} = 1.6 mA	Full			0.2	V
I_{OL} = 50 µA	Full			0.05	V

[1] Pull-up.
[2] Pull-down.

SWITCHING SPECIFICATIONS

Table 4.

Parameter	Symbol	Temperature	AD9250-170 Min	AD9250-170 Typ	AD9250-170 Max	AD9250-250 Min	AD9250-250 Typ	AD9250-250 Max	Unit
CLOCK INPUT PARAMETERS									
Conversion Rate[1]	f_S	Full	40		170	40		250	MSPS
SYSREF± Setup Time to Rising Edge CLK±[2]	t_{REFS}	Full		0.31			0.31		ns
SYSREF± Hold Time from Rising Edge CLK±[2]	t_{REFH}	Full		0			0		ns
SYSREF± Setup Time to Rising Edge RFCLK[2]	t_{REFSRF}	Full		0.50			0.50		ns
SYSREF± Hold Time from Rising Edge RFCLK[2]	t_{REFHRF}	Full		0			0		ns
CLK± Pulse Width High	t_{CH}								
Divide-by-1 Mode, DCS Enabled		Full	2.61	2.9	3.19	1.8	2.0	2.2	ns
Divide-by-1 Mode, DCS Disabled		Full	2.76	2.9	3.05	1.9	2.0	2.1	ns
Divide-by-2 Mode Through Divide-by-8 Mode		Full	0.8			0.8			ns
Aperture Delay	t_A	Full		1.0			1.0		ns
Aperture Uncertainty (Jitter)	t_J	Full		0.16			0.16		ps rms
DATA OUTPUT PARAMETERS									
Data Output Period or Unit Interval (UI)		Full		$L/(20 \times M \times f_S)$			$L/(20 \times M \times f_S)$		Seconds
Data Output Duty Cycle		25°C		50			50		%
Data Valid Time		25°C		0.84			0.78		UI
PLL Lock Time (t_{LOCK})		25°C		25			25		µs
Wake-Up Time									
Standby		25°C		10			10		µs
ADC (Power-Down)[3]		25°C		250			250		µs
Output (Power-Down)[4]		25°C		50			50		µs
SYNCINB± Falling Edge to First K.28 Characters		Full	4			4			Multiframes
CGS Phase K.28 Characters Duration		Full	1			1			Multiframe
Pipeline Delay									
JESD204B M1, L1 Mode (Latency)		Full		36			36		Cycles[5]
JESD204B M1, L2 Mode (Latency)		Full		59			59		Cycles
JESD204B M2, L1 Mode (Latency)		Full		25			25		Cycles
JESD204B M2, L2 Mode (Latency)		Full		36			36		Cycles
Fast Detect (Latency)		Full		7			7		Cycles
Data Rate per Lane		Full		3.4	5.0			5.0	Gbps
Uncorrelated Bounded High Probability (UBHP) Jitter		Full		6			8		ps
Random Jitter									
At 3.4 Gbps		Full		2.3					ps rms
At 5.0 Gbps		Full					1.7		ps rms
Output Rise/Fall Time		Full		60			60		ps
Differential Termination Resistance		25°C		100			100		Ω
Out-of-Range Recovery Time		Full		3			3		Cycles

[1] Conversion rate is the clock rate after the divider.
[2] Refer to Figure 3 for timing diagram.
[3] Wake-up time ADC is defined as the time required for the ADC to return to normal operation from power-down mode.
[4] Wake-up time output is defined as the time required for JESD204B output to return to normal operation from power-down mode.
[5] Cycles refers to ADC conversion rate cycles.

TIMING SPECIFICATIONS

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SPI TIMING REQUIREMENTS (See Figure 58)					
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between $\overline{CS}$ and SCLK	2			ns
t_H	Hold time between $\overline{CS}$ and SCLK	2			ns
t_{HIGH}	Minimum period that SCLK should be in a logic high state	10			ns
t_{LOW}	Minimum period that SCLK should be in a logic low state	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge (not shown in figures)	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge (not shown in figures)	10			ns
t_{SPI_RST}	Time required after hard or soft reset until SPI access is available (not shown in figures)	500			µs

Timing Diagrams

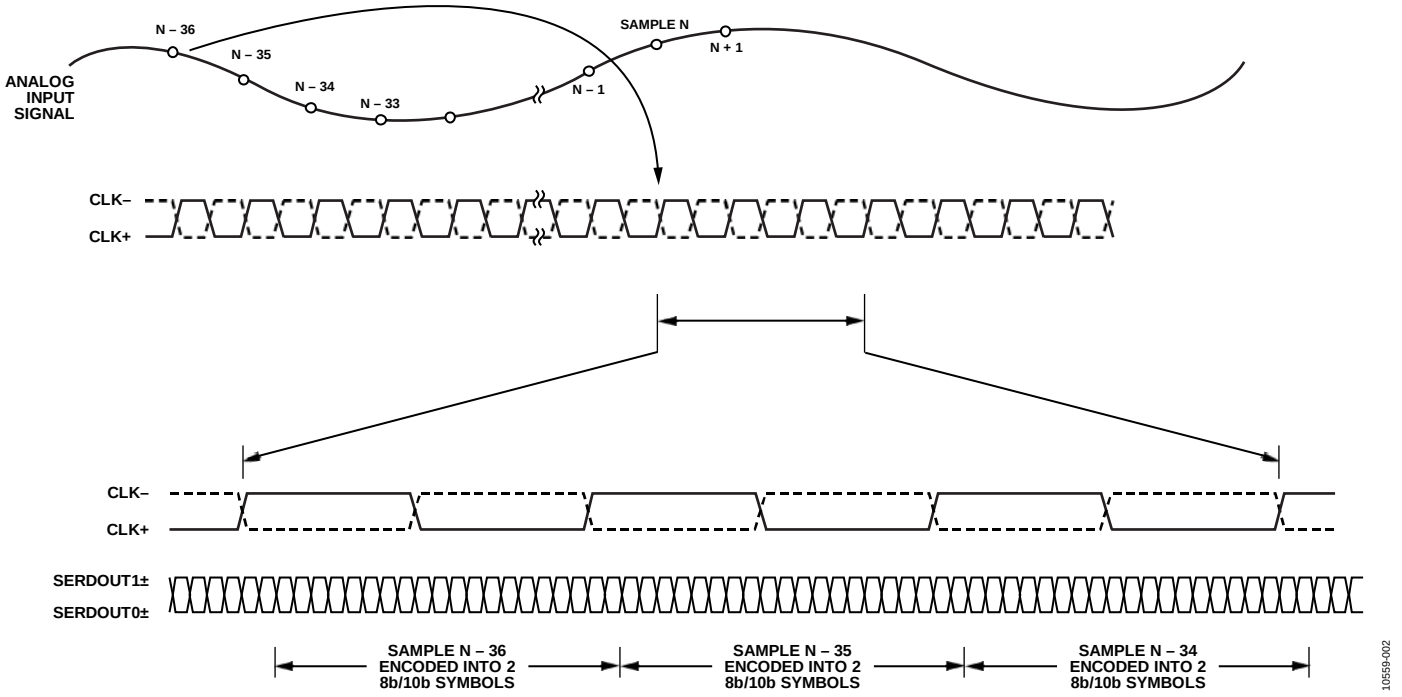

Figure 2. Data Output Timing

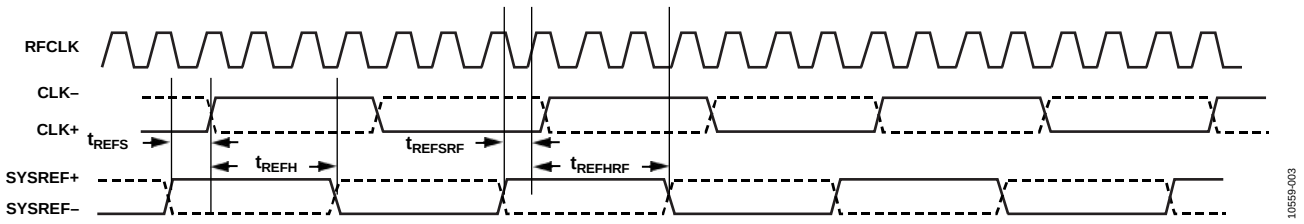

Figure 3. SYSREF± Setup and Hold Timing (Note that Clock Input is Either RFCLK or CLK±, Not Both)

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
ELECTRICAL	
AVDD to AGND	−0.3 V to +2.0 V
DRVDD to AGND	−0.3 V to +2.0 V
DVDD to DGND	−0.3 V to +2.0 V
VIN+A/VIN+B, VIN−A/VIN−B to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to AVDD + 0.2 V
RFCLK to AGND	−0.3 V to AVDD + 0.2 V
VCM to AGND	−0.3 V to AVDD + 0.2 V
$\overline{CS}$, PDWN to AGND	−0.3 V to AVDD + 0.3 V
SCLK to AGND	−0.3 V to AVDD + 0.3 V
SDIO to AGND	−0.3 V to AVDD + 0.3 V
$\overline{RST}$ to DGND	−0.3 V to DVDD + 0.3 V
FDA, FDB to DGND	−0.3 V to DVDD + 0.3 V
SERDOUT0+, SERDOUT0−, SERDOUT1+, SERDOUT1− to AGND	−0.3 V to DRVDD + 0.3 V
SYNCINB+, SYNCINB− to DGND	−0.3 V to DVDD + 0.3 V
SYSREF+, SYSREF− to AGND	−0.3 V to AVDD + 0.3 V
ENVIRONMENTAL	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

The exposed paddle must be soldered to the ground plane for the LFCSP package. This increases the reliability of the solder joints, maximizing the thermal capability of the package.

Table 7. Thermal Resistance

Package Type	Airflow Velocity (m/sec)	θ_{JA}[1,2]	θ_{JC}[1,3]	θ_{JB}[1,4]	Unit
48-Lead LFCSP 7 mm × 7 mm (CP-48-13)	0	25	2	14	°C/W
	1.0	22			°C/W
	2.5	20			°C/W

[1] Per JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-STD-883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Typical θ_{JA} is specified for a 4-layer printed circuit board (PCB) with a solid ground plane. As shown in Table 7, airflow increases heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes reduces the θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

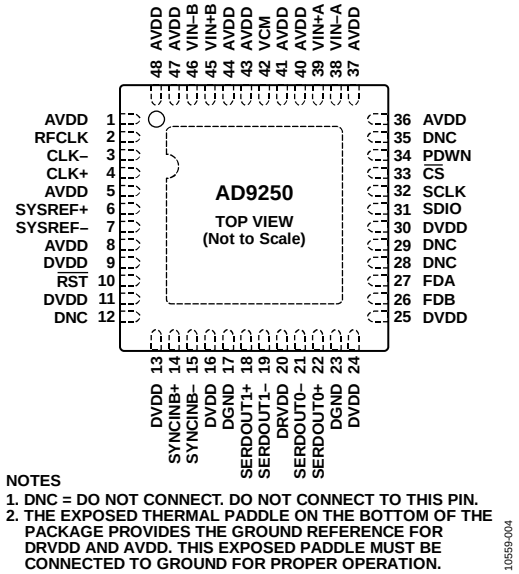

Figure 4. Pin Configuration (Top View)

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
1, 5, 8, 36, 37, 40, 41, 43, 44, 47, 48	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
9, 11, 13, 16, 24, 25, 30	DVDD	Supply	Digital Power Supply (1.8 V Nominal).
12, 28, 29, 35	DNC		Do Not Connect.
17, 23	DGND		Ground Reference for DVDD.
20	DRVDD	Supply	JESD204B PHY Serial Output Driver Supply (1.8 V Nominal). Note that the DRVDD power is referenced to the AGND Plane.
Exposed Paddle	AGND/DRGND	Ground	The exposed thermal paddle on the bottom of the package provides the ground reference for DRVDD and AVDD. This exposed paddle must be connected to ground for proper operation.
ADC Analog			
2	RFCLK	Input	ADC RF Clock Input.
3	CLK–	Input	ADC Nyquist Clock Input—Complement.
4	CLK+	Input	ADC Nyquist Clock Input—True.
38	VIN–A	Input	Differential Analog Input Pin (–) for Channel A.
39	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
42	VCM	Output	Common-Mode Level Bias Output for Analog Inputs. Decouple this pin to ground using a 0.1 µF capacitor.
45	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
46	VIN–B	Input	Differential Analog Input Pin (–) for Channel B.
ADC Fast Detect Outputs			
26	FDB	Output	Channel B Fast Detect Indicator (CMOS Levels).
27	FDA	Output	Channel A Fast Detect Indicator (CMOS Levels).
Digital Inputs			
6	SYSREF+	Input	JESD204B LVDS SYSREF Input—True
7	SYSREF–	Input	JESD204B LVDS SYSREF Input—Complement.
14	SYNCINB+	Input	JESD204B LVDS SYNC Input—True
15	SYNCINB–	Input	JESD204B LVDS SYNC Input—Complement.

Pin No.	Mnemonic	Type	Description
Data Outputs			
18	SERDOUT1+	Output	Lane B CML Output Data—True.
19	SERDOUT1−	Output	Lane B CML Output Data—Complement.
21	SERDOUT0−	Output	Lane A CML Output Data—Complement.
22	SERDOUT0+	Output	Lane A CML Output Data—True.
DUT Controls			
10	$\overline{\text{RST}}$	Input	Digital Reset (Active Low).
31	SDIO	Input/Output	SPI Serial Data I/O.
32	SCLK	Input	SPI Serial Clock.
33	$\overline{\text{CS}}$	Input	SPI Chip Select (Active Low).
34	PDWN	Input	Power-Down Input (Active High). The operation of this pin depends on the SPI mode and can be configured as power-down or standby (see Table 17).

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V, DRVDD = 1.8 V, DVDD = 1.8 V, sample rate is maximum for speed grade, DCS enabled, 1.75 V p-p differential input, VIN = −1.0 dBFS, 32k sample, T_A = 25°C, link parameters used were M = 2 and L = 2, unless otherwise noted.

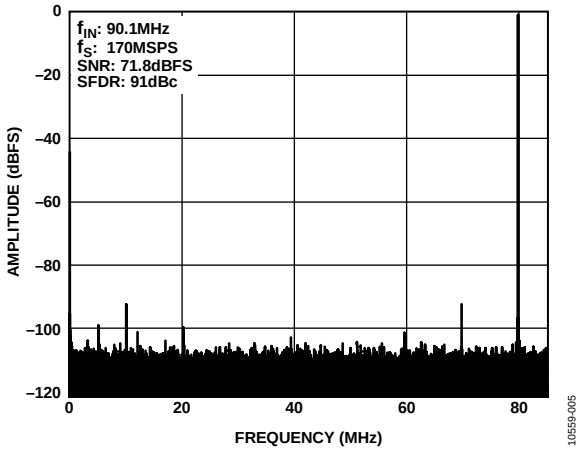

Figure 5. AD9250-170 Single-Tone FFT with f_{IN} = 90.1 MHz

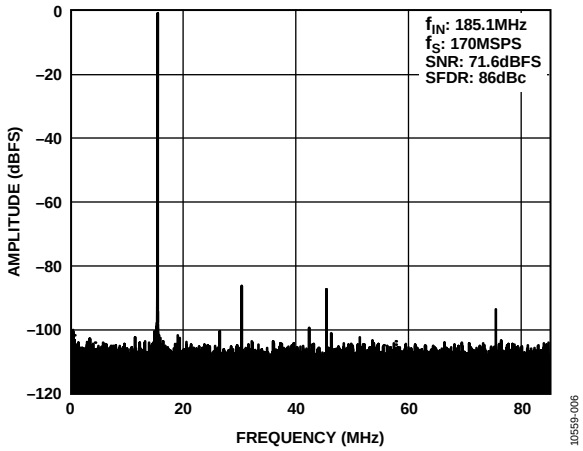

Figure 6. AD9250-170 Single-Tone FFT with f_{IN} = 185.1 MHz

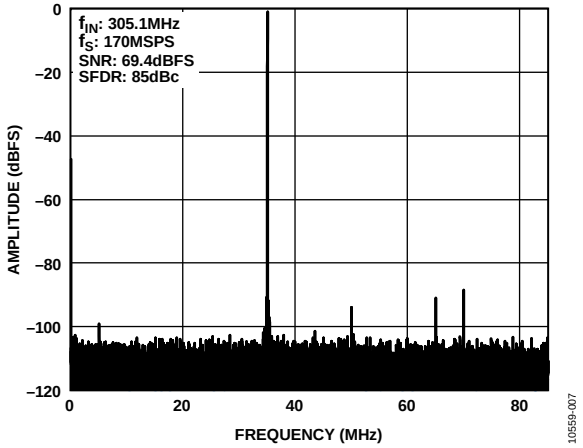

Figure 7. AD9250-170 Single-Tone FFT with f_{IN} = 305.1 MHz

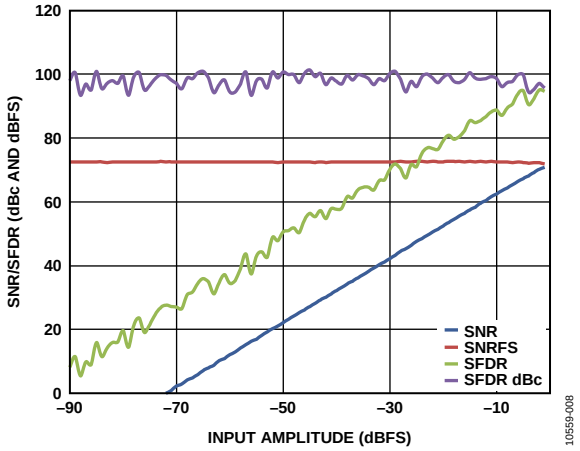

Figure 8. AD9250-170 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 185.1 MHz

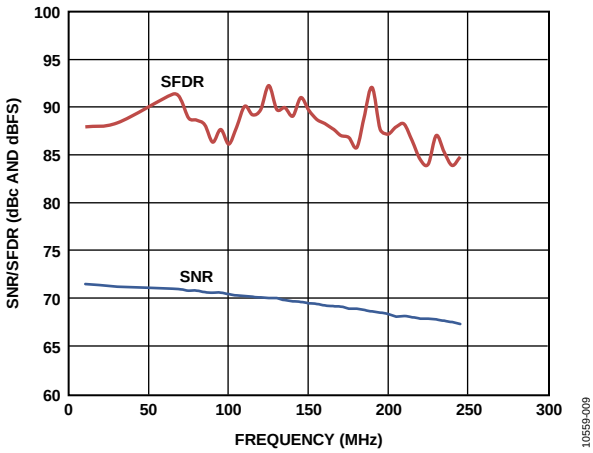

Figure 9. AD9250-170 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN})

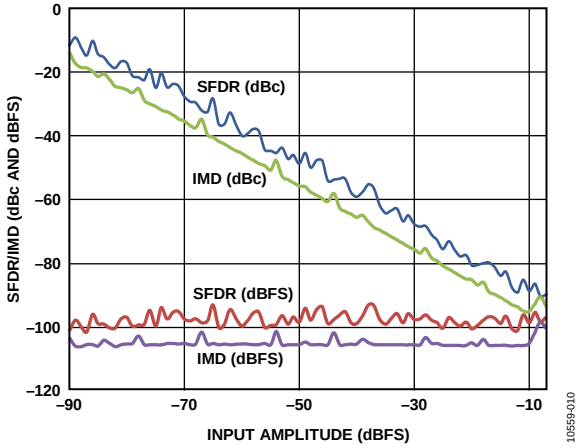

Figure 10. AD9250-170 Two-Tone SFDR/IMD vs. Input Amplitude (A_{IN}) with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz, f_S = 170 MSPS

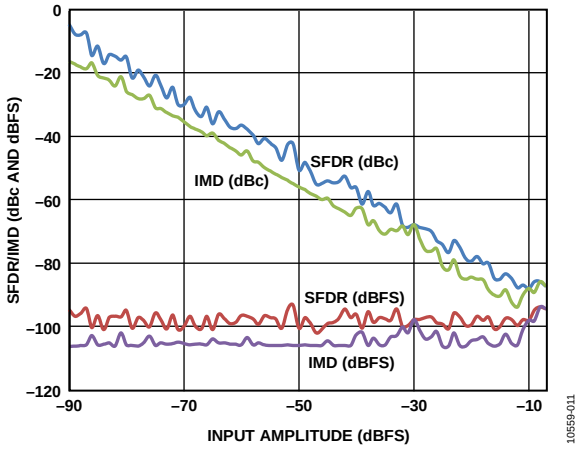

Figure 11. AD9250-170 Two-Tone SFDR/IMD vs. Input Amplitude (A_{IN}) with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz, f_S = 170 MSPS

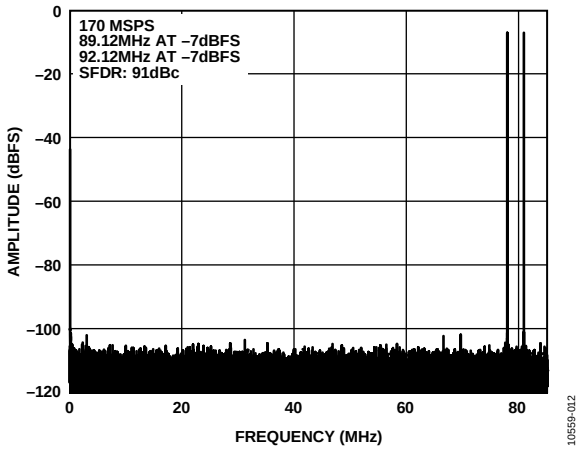

Figure 12. AD9250-170 Two-Tone FFT with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz, f_S = 170 MSPS

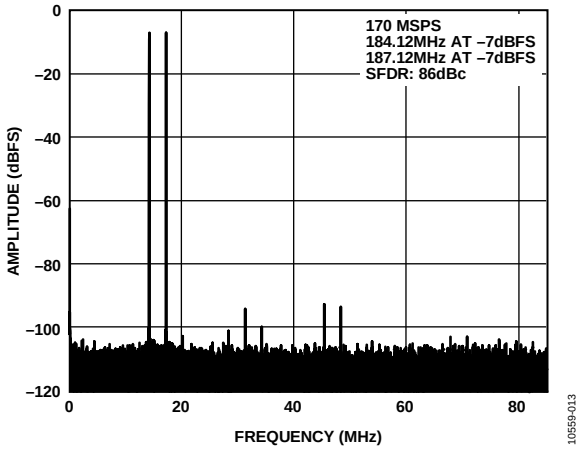

Figure 13. AD9250-170 Two-Tone FFT with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz, f_S = 170 MSPS

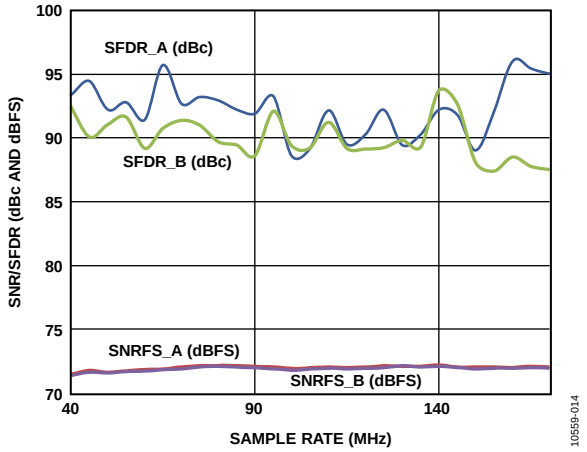

Figure 14. AD9250-170 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 90.1 MHz

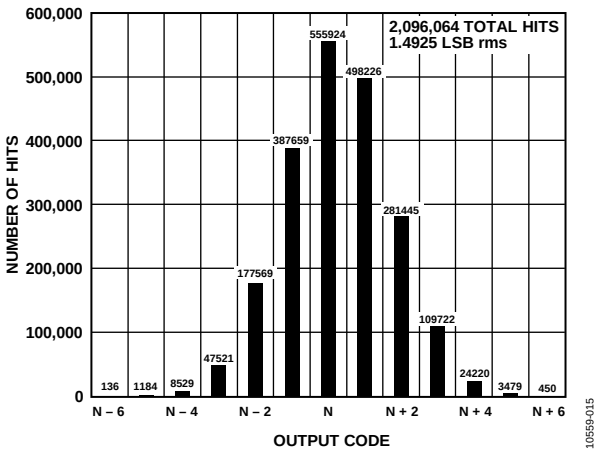

Figure 15. AD9250-170 Grounded Input Histogram

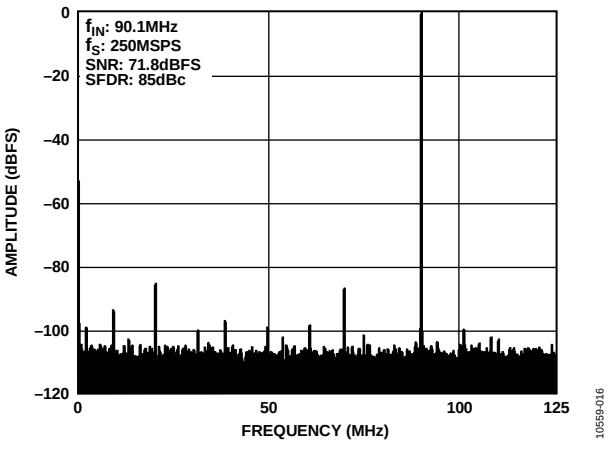

Figure 16. AD9250-250 Single-Tone FFT with f_{IN} = 90.1 MHz

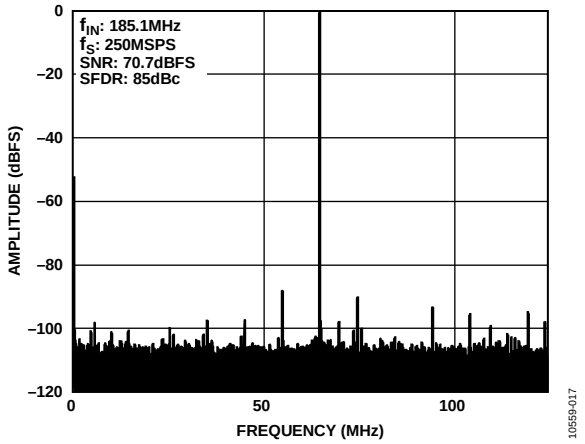

Figure 17. AD9250-250 Single-Tone FFT with f_{IN} = 185.1 MHz

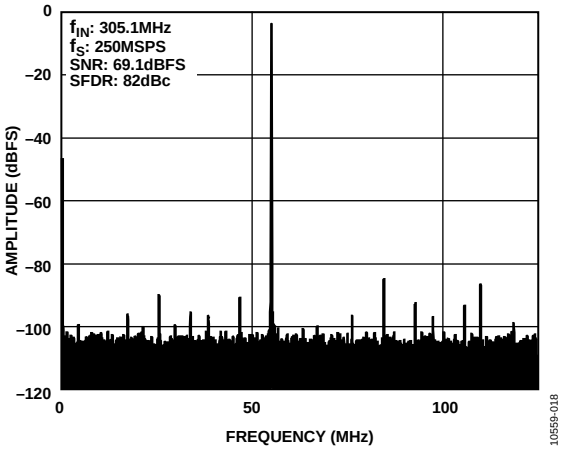

Figure 18. AD9250-250 Single-Tone FFT with f_{IN} = 305.1 MHz

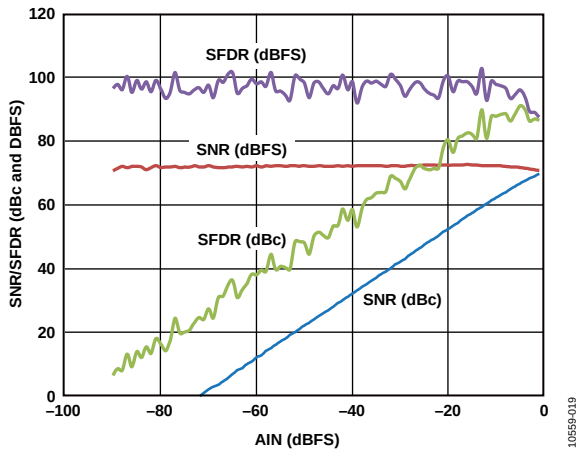

Figure 19. AD9250-250 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 185.1 MHz

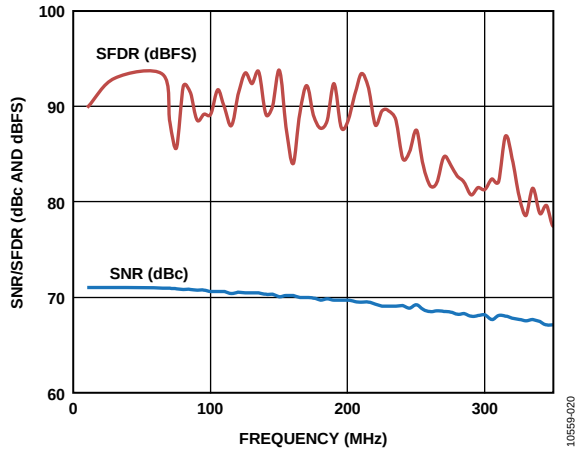

Figure 20. AD9250-250 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN})

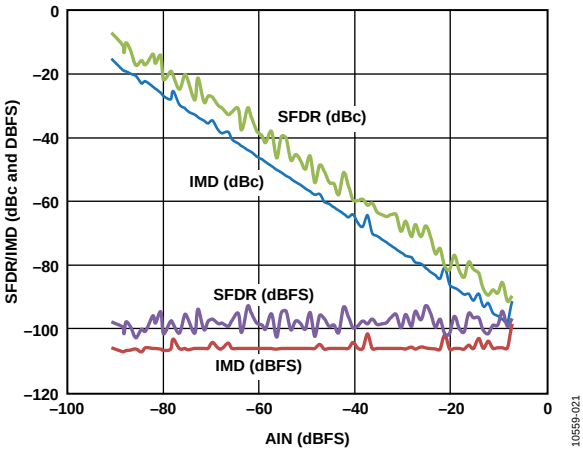

Figure 21. AD9250-250 Two-Tone SFDR/IMD vs. Input Amplitude (A_{IN}) with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz, f_S = 250 MSPS

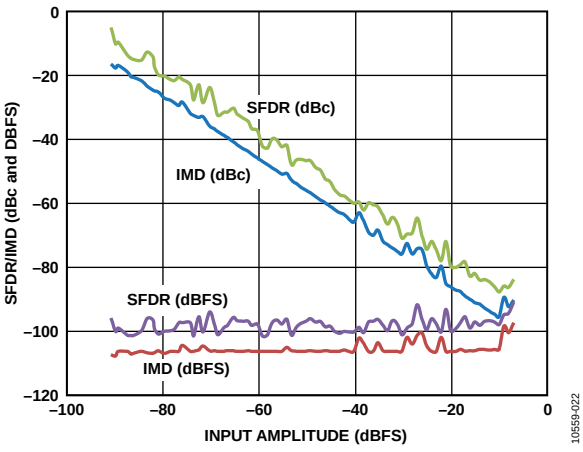

Figure 22. AD9250-250 Two-Tone SFDR/IMD vs. Input Amplitude (A_{IN}) with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz, f_S = 250 MSPS

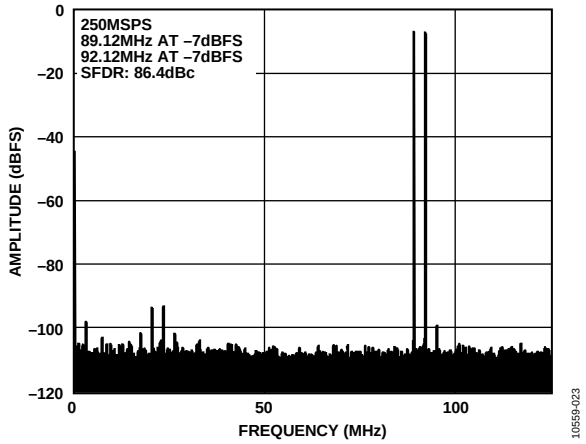

Figure 23. AD9250-250 Two-Tone FFT with f_{IN1} = 89.12 MHz, f_{IN2} = 92.12 MHz, f_S = 250 MSPS

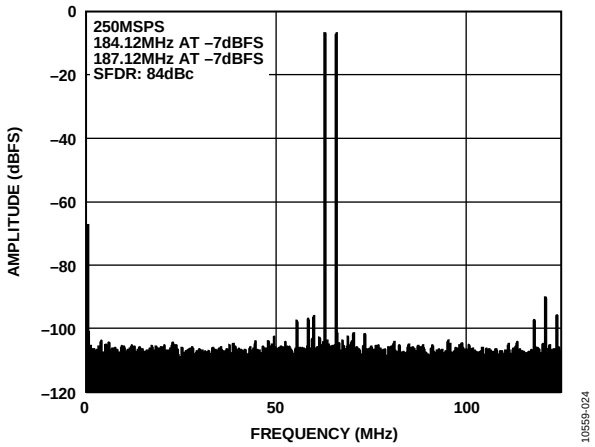

Figure 24. AD9250-250 Two-Tone FFT with f_{IN1} = 184.12 MHz, f_{IN2} = 187.12 MHz, f_S = 250 MSPS

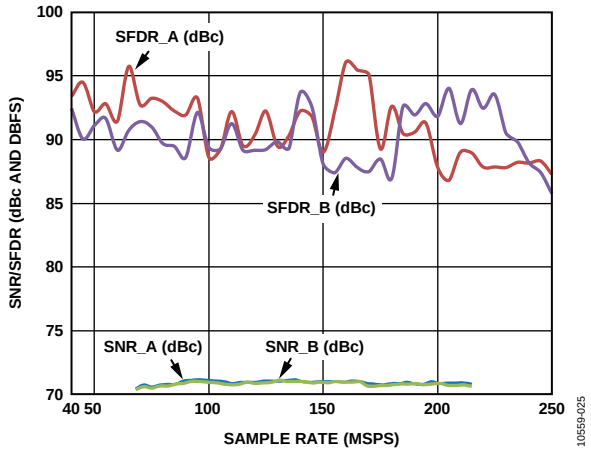

Figure 25. AD9250-250 Single-Tone SNR/SFDR vs. Sample Rate (f_S) with f_{IN} = 90.1 MHz

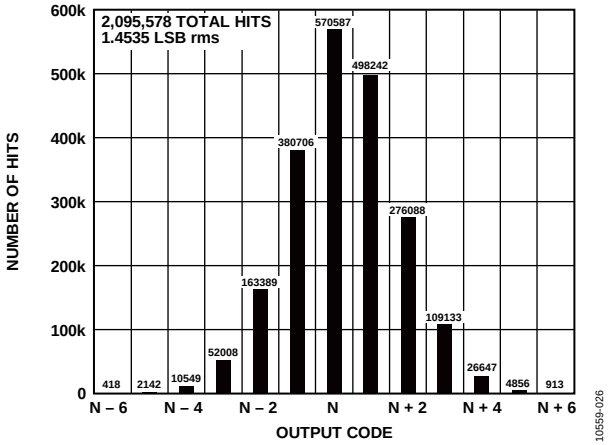

Figure 26. AD9250-250 Grounded Input Histogram

EQUIVALENT CIRCUITS

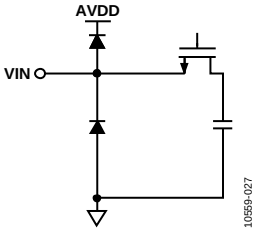

Figure 27. Equivalent Analog Input Circuit

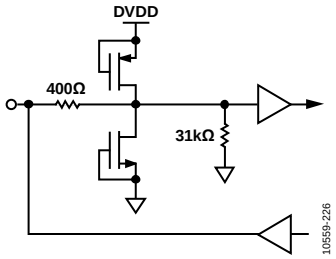

Figure 31. Equivalent SDIO Circuit

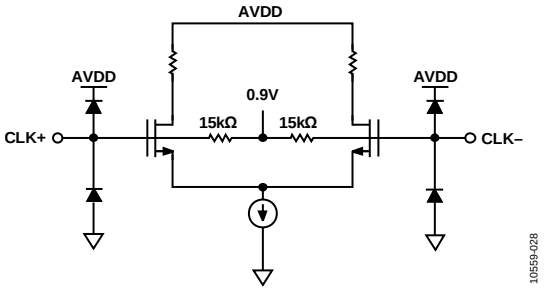

Figure 28. Equivalent Clock Input Circuit

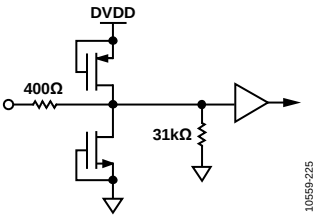

Figure 32. Equivalent SCLK or PDWN Input Circuit

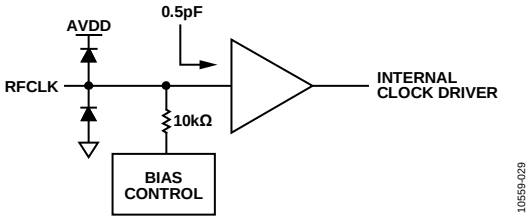

Figure 29. Equivalent RF Clock Input Circuit

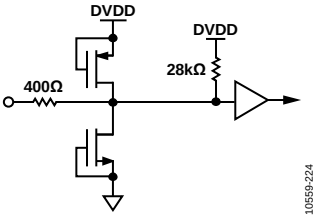

Figure 33. Equivalent $\overline{CS}$ or $\overline{RST}$ Input Circuit

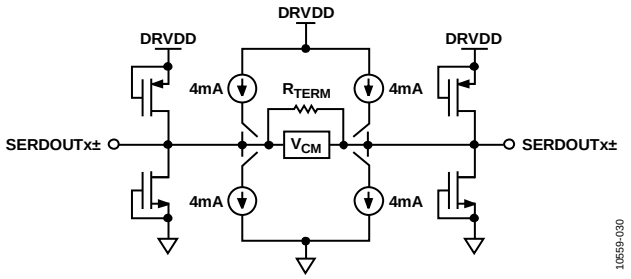

Figure 30. Digital CML Output Circuit

THEORY OF OPERATION

The AD9250 has two analog input channels and two JESD204B output lanes. The signal passes through several stages before appearing at the output port(s).

The dual ADC design can be used for diversity reception of signals, where the ADCs operate identically on the same carrier but from two separate antennae. The ADCs can also be operated with independent analog inputs. The user can sample frequencies from dc to 300 MHz using appropriate low-pass or band-pass filtering at the ADC inputs with little loss in ADC performance. Operation to 400 MHz analog input is permitted but occurs at the expense of increased ADC noise and distortion.

A synchronization capability is provided to allow synchronized timing between multiple devices.

Programming and control of the AD9250 are accomplished using a 3-pin, SPI-compatible serial interface.

ADC ARCHITECTURE

The AD9250 architecture consists of a dual, front-end, sample-and-hold circuit, followed by a pipelined switched capacitor ADC. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample and the remaining stages to operate on the preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor digital-to-analog converter (DAC) and an interstage residue amplifier (MDAC). The MDAC magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage of each channel contains a differential sampling circuit that can be ac- or dc-coupled in differential or single-ended modes. The output staging block aligns the data, corrects errors, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing digital output noise to be separated from the analog core.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9250 is a differential, switched capacitor circuit that has been designed for optimum performance while processing a differential input signal.

The clock signal alternatively switches the input between sample mode and hold mode (see the configuration shown in Figure 34). When the input is switched into sample mode, the signal source must be capable of charging the sampling capacitors and settling within 1/2 clock cycle.

A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. A shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC input; therefore, the precise values are dependent on the application.

In intermediate frequency (IF) undersampling applications, reduce the shunt capacitors. In combination with the driving source impedance, the shunt capacitors limit the input bandwidth. Refer to the AN-742 Application Note, *Frequency Domain Response of Switched-Capacitor ADCs*; the AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*; and the *Analog Dialogue* article, "Transformer-Coupled Front-End for Wideband A/D Converters," for more information on this subject.

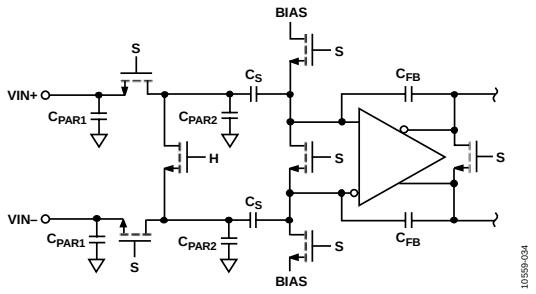

Figure 34. Switched-Capacitor Input

For best dynamic performance, match the source impedances driving VIN+ and VIN− and differentially balance the inputs.

Input Common Mode

The analog inputs of the AD9250 are not internally dc biased. In ac-coupled applications, the user must provide this bias externally. Setting the device so that V_{CM} = 0.5 × AVDD (or 0.9 V) is recommended for optimum performance. An on-board common-mode voltage reference is included in the design and is available from the VCM pin. Using the VCM output to set the input common mode is recommended. Optimum performance is achieved when the common-mode voltage of the analog input is set by the VCM pin voltage (typically 0.5 × AVDD). Decouple the VCM pin to ground by using a 0.1 µF capacitor, as described in the Applications Information section. Place this decoupling capacitor close to the pin to minimize the series resistance and inductance between the part and this capacitor.

Differential Input Configurations

Optimum performance is achieved while driving the AD9250 in a differential input configuration. For baseband applications, the AD8138, ADA4937-2, ADA4938-2, and ADA4930-2 differential drivers provide excellent performance and a flexible interface to the ADC.

The output common-mode voltage of the ADA4930-2 is easily set with the VCM pin of the AD9250 (see Figure 35), and the driver can be configured in a Sallen-Key filter topology to provide band-limiting of the input signal.

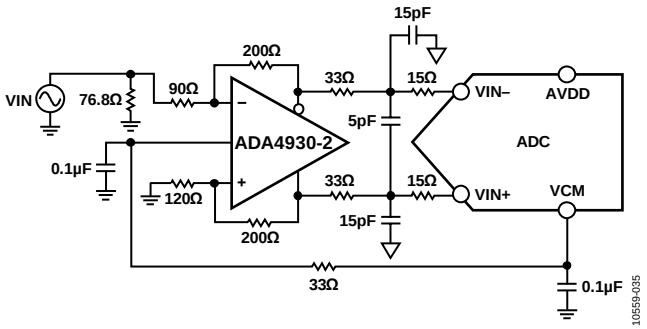

Figure 35. Differential Input Configuration Using the ADA4930-2

For baseband applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example is shown in Figure 36. To bias the analog input, the VCM voltage can be connected to the center tap of the secondary winding of the transformer.

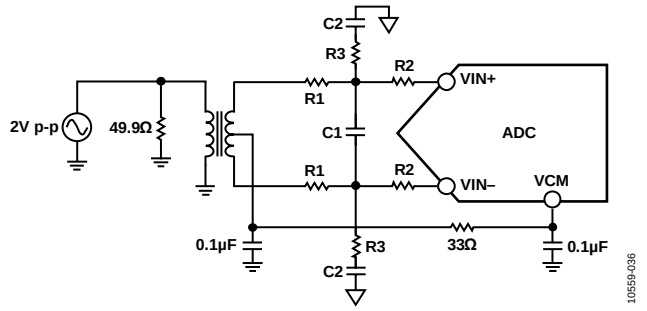

Figure 36. Differential Transformer-Coupled Configuration

Consider the signal characteristics when selecting a transformer. Most RF transformers saturate at frequencies below a few megahertz. Excessive signal power can also cause core saturation, which leads to distortion.

At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD9250. For applications where SNR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 37). In this configuration, the input is ac-coupled and the VCM voltage is provided to each input through a 33 Ω resistor. These resistors compensate for losses in the input baluns to provide a 50 Ω impedance to the driver.

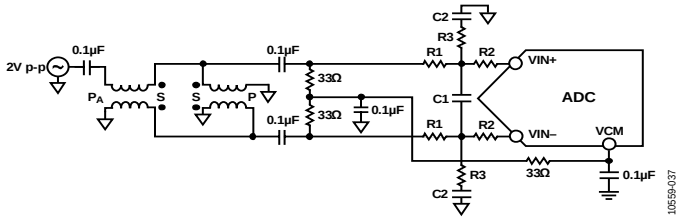

Figure 37. Differential Double Balun Input Configuration

In the double balun and transformer configurations, the value of the input capacitors and resistors is dependent on the input frequency and source impedance. Based on these parameters, the value of the input resistors and capacitors may need to be adjusted or some components may need to be removed. Table 9 displays recommended values to set the RC network for different input frequency ranges. However, these values are dependent on the input signal and bandwidth and should be used only as a starting guide. Note that the values given in Table 9 are for each R1, R2, C1, C2, and R3 components shown in Figure 36 and Figure 37.

Table 9. Example RC Network

Frequency Range (MHz)	R1 Series (Ω)	C1 Differential (pF)	R2 Series (Ω)	C2 Shunt (pF)	R3 Shunt (Ω)
0 to 100	33	8.2	0	15	49.9
100 to 300	15	3.9	0	8.2	49.9

An alternative to using a transformer-coupled input at frequencies in the second Nyquist zone is to use an amplifier with variable gain. The AD8375 or AD8376 digital variable gain amplifier (DVGAs) provides good performance for driving the AD9250. Figure 38 shows an example of the AD8376 driving the AD9250 through a band-pass antialiasing filter.

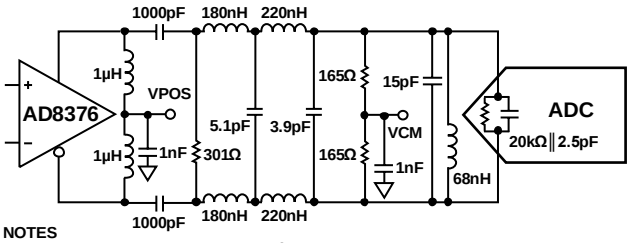

Figure 38. Differential Input Configuration Using the AD8376

VOLTAGE REFERENCE

A stable and accurate voltage reference is built into the AD9250. The full-scale input range can be adjusted by varying the reference voltage via the SPI. The input span of the ADC tracks the reference voltage changes linearly.

CLOCK INPUT CONSIDERATIONS

The AD9250 has two options for deriving the input sampling clock, a differential Nyquist sampling clock input or an RF clock input (which is internally divided by 4). The clock input is selected in Register 0x09 and by default is configured for the Nyquist clock input. For optimum performance, clock the AD9250 Nyquist sample clock input, CLK+ and CLK–, with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK– pins via a transformer or via capacitors. These pins are biased internally (see Figure 39) and require no external bias. If the clock inputs are floated, CLK– is pulled slightly lower than CLK+ to prevent spurious clocking.

Nyquist Clock Input Options

The AD9250 Nyquist clock input supports a differential clock between 40 MHz to 625 MHz. The clock input structure supports differential input voltages from 0.3 V to 3.6 V and is therefore compatible with various logic family inputs, such as CMOS, LVDS, and LVPECL. A sine wave input is also accepted, but higher slew rates typically provide optimal performance. Clock source jitter is a critical parameter that can affect performance, as described in the Jitter Considerations section. If the inputs are floated, pull the CLK– pin low to prevent spurious clocking.

The Nyquist clock input pins, CLK+ and CLK–, are internally biased to 0.9 V and have a typical input impedance of 4 pF in parallel with 10 kΩ (see Figure 39). The input clock is typically ac-coupled to CLK+ and CLK–. Some typical clock drive circuits are presented in Figure 40 through Figure 43 for reference.

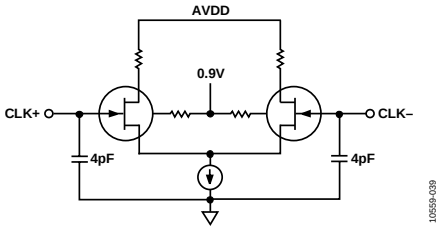

Figure 39. Equivalent Nyquist Clock Input Circuit

For applications where a single-ended low jitter clock between 40 MHz to 200 MHz is available, an RF transformer is recommended. An example using an RF transformer in the clock network is shown in Figure 40. At frequencies above 200 MHz, an RF balun is recommended, as seen in Figure 41. The back-to-back Schottky diodes across the transformer secondary limit clock excursions into the AD9250 to approximately 0.8 V p-p differential. This limit helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9250, yet preserves the fast rise and fall times of the clock, which are critical to low jitter performance.

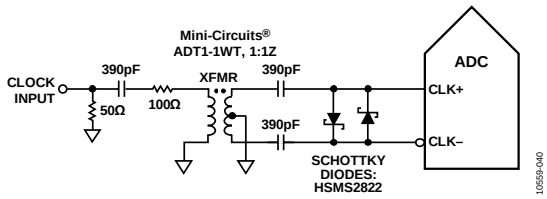

Figure 40. Transformer-Coupled Differential Clock (Up to 200 MHz)

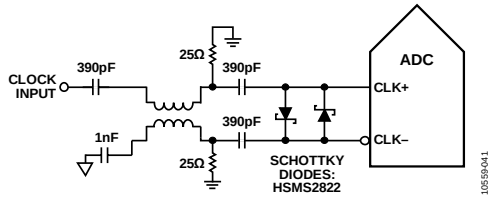

Figure 41. Balun-Coupled Differential Clock (Up to 625 MHz)

In some cases, it is desirable to buffer or generate multiple clocks from a single source. In those cases, Analog Devices, Inc., offers clock drivers with excellent jitter performance. Figure 42 shows a typical PECL driver circuit that uses PECL drivers such as the AD9510, AD9511, AD9512, AD9513, AD9514, AD9515, AD9516, AD9517, AD9518, AD9520, AD9522, AD9523, AD9524, and ADCLK905, ADCLK907, and ADCLK925.

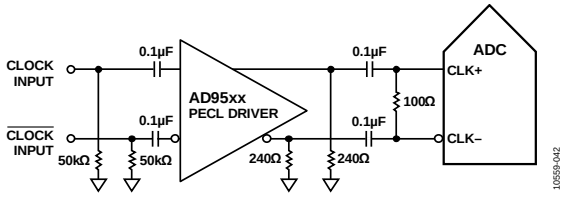

Figure 42. Differential PECL Sample Clock (Up to 625 MHz)

Analog Devices also offers LVDS clock drivers with excellent jitter performance. A typical circuit is shown in Figure 43 and uses LVDS drivers such as the AD9510, AD9511, AD9512, AD9513, AD9514, AD9515, AD9516, AD9517, AD9518, AD9520, AD9522, AD9523, and AD9524.

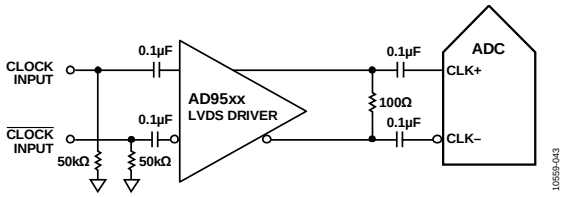

Figure 43. Differential LVDS Sample Clock (Up to 625 MHz)

RF Clock Input Options

The AD9250 RF clock input supports a single-ended clock between 625 GHz to 1.5 GHz. The equivalent RF clock input circuit is shown in Figure 44. The input is self biased to 0.9 V and is typically ac-coupled. The input has a typical input impedance of 10 kΩ in parallel with 1 pF at the RFCLK pin.

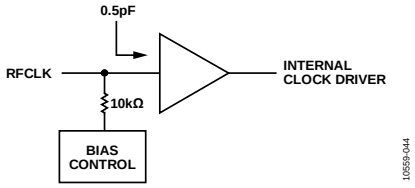

Figure 44. Equivalent RF Clock Input Circuit

It is recommended to drive the RF clock input of the AD9250 with a PECL or sine wave signal with a minimum signal amplitude of 600 mV peak to peak. Regardless of the type of signal being used, clock source jitter is of the most concern, as described in the Jitter Considerations section. Figure 45 shows the preferred method of clocking when using the RF clock input on the AD9250. It is recommended to use a 50 Ω transmission line to route the clock signal to the RF clock input of the AD9250 due to the high frequency nature of the signal and terminate the transmission line close to the RF clock input.

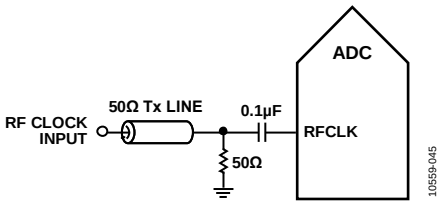

Figure 45. Typical RF Clock Input Circuit

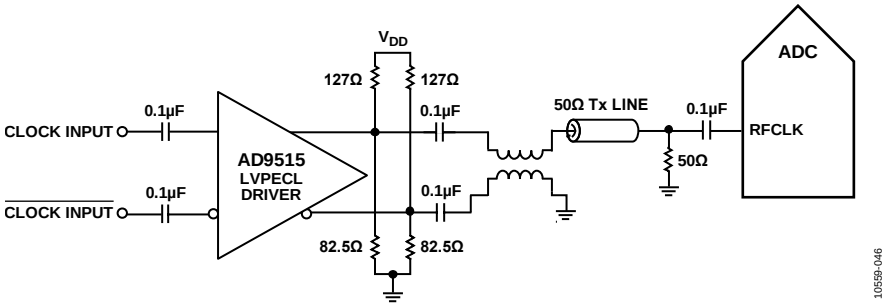

Figure 46. Differential PECL RF Clock Input Circuit

Figure 46 shows the RF clock input of the AD9250 being driven from the LVPECL outputs of the AD9515. The differential LVPECL output signal from the AD9515 is converted to a single-ended signal using an RF balun or RF transformer. The RF balun configuration is recommended for clock frequencies associated with the RF clock input.

Input Clock Divider

The AD9250 contains an input clock divider with the ability to divide the Nyquist input clock by integer values between 1 and 8. The RF clock input uses an on-chip predivider to divide the clock input by four before it reaches the 1 to 8 divider. This allows higher input frequencies to be achieved on the RF clock input. The divide ratios can be selected using Register 0x09 and Register 0x0B. Register 0x09 is used to set the RF clock input, and Register 0x0B can be used to set the divide ratio of the 1-to-8 divider for both the RF clock input and the Nyquist clock input. For divide ratios other than 1, the duty-cycle stabilizer is automatically enabled.

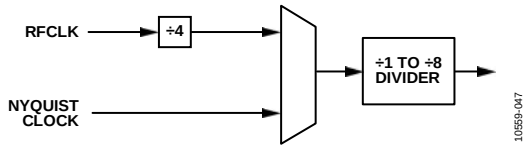

Figure 47. AD9250 Clock Divider Circuit

The AD9250 clock divider can be synchronized using the external SYSREF input. Bit 1 and Bit 2 of Register 0x3A allow the clock divider to be resynchronized on every SYSREF signal or only on the first signal after the register is written. A valid SYSREF causes the clock divider to reset to its initial state. This synchronization feature allows multiple parts to have their clock dividers aligned to guarantee simultaneous input sampling.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9250 contains a DCS that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD9250.

Jitter on the rising edge of the input clock is still of paramount concern and is not reduced by the duty cycle stabilizer. The duty cycle control loop does not function for clock rates less than 40 MHz nominally. The loop has a time constant associated with it that must be considered when the clock rate can change dynamically. A wait time of 1.5 µs to 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal. During the time that the loop is not locked, the DCS loop is bypassed, and the internal device timing is dependent on the duty cycle of the input clock signal. In such applications, it may be appropriate to disable the duty cycle stabilizer. In all other applications, enabling the DCS circuit is recommended to maximize ac performance.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given input frequency (f_{IN}) due to jitter (t_J) can be calculated by

$$SNR_{HF} = -10 \log[(2\pi \times f_{IN} \times t_{JRMS})^2 + 10^{(-SNR_{LF}/10)}]$$

In the equation, the rms aperture jitter represents the root-mean-square of all jitter sources, which include the clock input, the analog input signal, and the ADC aperture jitter specification. IF undersampling applications are particularly sensitive to jitter, as shown in Figure 48.

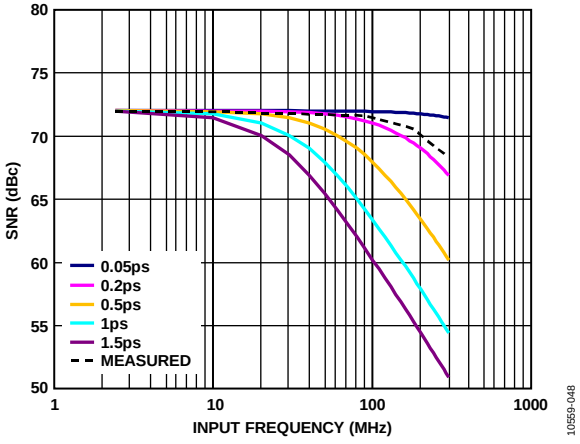

Figure 48. AD9250-250 SNR vs. Input Frequency and Jitter

Treat the clock input as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9250. Separate the power supplies for the clock drivers from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or another method), retime it by the original clock at the last step.

Refer to the AN-501 Application Note, *Aperture Uncertainty and ADC System Performance*, and the AN-756 Application Note, *Sampled Systems and the Effects of Clock Phase Noise and Jitter*, for more information about jitter performance as it relates to ADCs.

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 49, the power dissipated by the AD9250 is proportional to its sample rate. The data in Figure 49 was taken using the same operating conditions as those used for the Typical Performance Characteristics section.

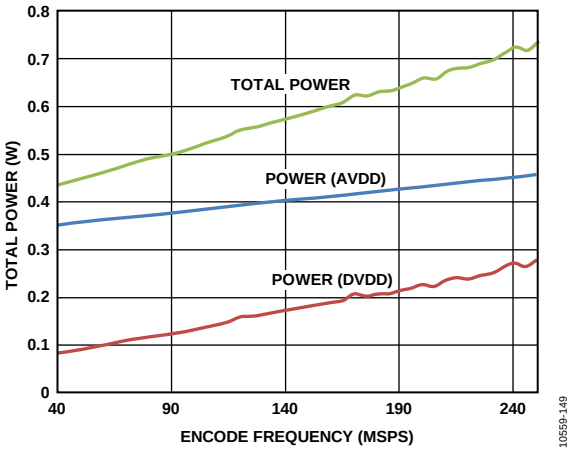

Figure 49. AD9250-250 Power vs. Encode Rate

By asserting PDWN (either through the SPI port or by asserting the PDWN pin high), the AD9250 is placed in power-down mode. In this state, the ADC typically dissipates about 9 mW. Asserting the PDWN pin low returns the AD9250 to its normal operating mode.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. Internal capacitors are discharged when entering power-down mode and then must be recharged when returning to normal operation. As a result, wake-up time is related to the time spent in power-down mode, and shorter power-down cycles result in proportionally shorter wake-up times.

When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the Memory Map Register Description section and the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, for additional details.

DIGITAL OUTPUTS

JESD204B Transmit Top Level Description

The AD9250 digital output uses the JEDEC Standard No. JESD204B, *Serial Interface for Data Converters*. JESD204B is a protocol to link the AD9250 to a digital processing device over a serial interface of up to 5 Gbps link speeds (3.5 Gbps, 14-bit ADC data rate). The benefits of the JESD204B interface include a reduction in required board area for data interface routing and the enabling of smaller packages for converter and logic devices. The AD9250 supports single or dual lane interfaces.

JESD204B Overview

The JESD204B data transmit block assembles the parallel data from the ADC into frames and uses 8b/10b encoding as well as optional scrambling to form serial output data. Lane synchronization is supported using special characters during the initial establishment of the link, and additional synchronization is embedded in the data stream thereafter. A matching external receiver is required to lock onto the serial data stream and recover the data and clock. For additional details on the JESD204B interface, refer to the JESD204B standard.

The AD9250 JESD204B transmit block maps the output of the two ADCs over a link. A link can be configured to use either single or dual serial differential outputs that are called lanes. The JESD204B specification refers to a number of parameters to define the link, and these parameters must match between the JESD204B transmitter (AD9250 output) and receiver.

The JESD204B link is described according to the following parameters:

- S = samples transmitted/single converter/frame cycle (AD9250 value = 1)
- M = number of converters/converter device (AD9250 value = 2 by default, or can be set to 1)
- L = number of lanes/converter device (AD9250 value = 1 or 2)
- N = converter resolution (AD9250 value = 14)
- N' = total number of bits per sample (AD9250 value = 16)
- CF = number of control words/frame clock cycle/converter device (AD9250 value = 0)
- CS = number of control bits/conversion sample (configurable on the AD9250 up to 2 bits)
- K = number of frames per multiframe (configurable on the AD9250)
- HD = high density mode (AD9250 value = 0)
- F = octets/frame (AD9250 value = 2 or 4, dependent upon L = 2 or 1)
- C = control bit (overrange, overflow, underflow; available on the AD9250)
- T = tail bit (available on the AD9250)
- SCR = scrambler enable/disable (configurable on the AD9250)
- FCHK = checksum for the JESD204B parameters (automatically calculated and stored in register map)

Figure 50 shows a simplified block diagram of the AD9250 JESD204B link. By default, the AD9250 is configured to use two converters and two lanes. Converter A data is output to SERDOUT0+/SERDOUT0−, and Converter B is output to SERDOUT1+/SERDOUT1−. The AD9250 allows for other configurations such as combining the outputs of both converters onto a single lane or changing the mapping of the A and B digital output paths. These modes are setup through a quick configuration register in the SPI register map, along with additional customizable options.

By default in the AD9250, the 14-bit converter word from each converter is broken into two octets (8 bits of data). Bit 0 (MSB) through Bit 7 are in the first octet. The second octet contains Bit 8 through Bit 13 (LSB) and two tail bits. The tail bits can be configured as zeros, pseudo-random number sequence or control bits indicating overrange, underrange, or valid data conditions.

The two resulting octets can be scrambled. Scrambling is optional; however, it is available to avoid spectral peaks when transmitting similar digital data patterns. The scrambler uses a self synchronizing, polynomial-based algorithm defined by the equation $1 + x^{14} + x^{15}$. The descrambler in the receiver should be a self-synchronizing version of the scrambler polynomial.

The two octets are then encoded with an 8b/10b encoder. The 8b/10b encoder works by taking eight bits of data (an octet) and encoding them into a 10-bit symbol. Figure 51 shows how the 14-bit data is taken from the ADC, the tail bits are added, the two octets are scrambled, and how the octets are encoded into two 10-bit symbols. Figure 51 illustrates the default data format.

At the data link layer, in addition to the 8b/10b encoding, the character replacement is used to allow the receiver to monitor frame alignment. The character replacement process occurs on the frame and multiframe boundaries, and implementation depends on which boundary is occurring, and if scrambling is enabled.

If scrambling is disabled, the following applies. If the last scrambled octet of the last frame of the multiframe equals the last octet of the previous frame, the transmitter replaces the last octet with the control character /A/ = /K28.3/. On other frames within the multiframe, if the last octet in the frame equals the last octet of the previous frame, the transmitter replaces the last octet with the control character /F/= /K28.7/.

If scrambling is enabled, the following applies. If the last octet of the last frame of the multiframe equals 0x7C, the transmitter replaces the last octet with the control character /A/ = /K28.3/. On other frames within the multiframe, if the last octet equals 0xFC, the transmitter replaces the last octet with the control character /F/ = /K28.7/.

Refer to JEDEC Standard No. 204B-July 2011 for additional information about the JESD204B interface. Section 5.1 covers the transport layer and data format details and Section 5.2 covers scrambling and descrambling.

JESD204B Synchronization Details

The AD9250 supports JESD204B Subclass 0 and Subclass 1 and establishes synchronization of the link through one or two control signals, SYNC and Subclass 1 also use SYSREF, and a common device clock. SYSREF and SYNC are common to all converter devices for alignment purposes at the system level.

The synchronization process is accomplished over three phases: code group synchronization (CGS), initial lane alignment sequence (ILAS), and data transmission. If scrambling is enabled, scrambling begins with the first data byte following the last alignment character of the ILAS. CGS and ILAS phases are not scrambled.

CGS Phase

In the CGS phase, the JESD204B transmit block transmits /K28.5/ characters. The receiver (external logic device) must locate K28.5 characters in its input data stream using clock and data recovery (CDR) techniques.

When in Subclass 1 mode, the receiver locks onto the K28.5 characters. Once detected, the receiver initiates a SYSREF edge so that the AD9250 transmit data establishes a local multiframe clock (LMFC) internally.

The SYSREF edge also resets any sampling edges within the ADC to align sampling instances to the LMFC. This is important to maintain synchronization across multiple devices.

If Subclass 0: at the next receiver's internal clock; if Subclass 1: at the next receiver's LMFC boundary, the receiver or logic device de-asserts the SYNC~ signal (SYNCINB± goes high), and the transmitter block begins the ILAS phase.

ILAS Phase

In the ILAS phase, the transmitter sends out a known pattern, and the receiver aligns all lanes of the link and verifies the parameters of the link.

The ILAS phase begins after SYNC~ has been de-asserted (goes high). If Subclass 0: the transmitter begins ILAS at the next transmitter's internal clock; if Subclass 1: at the next transmitter's internal LMFC boundary, the transmit block begins to transmit four multiframes. Dummy samples are inserted between the required characters so that full multiframes are transmitted. The four multiframes include the following:

- Multiframe 1: Begins with an /R/ character [K28.0] and ends with an /A/ character [K28.3].
- Multiframe 2: Begins with an /R/ character followed by a /Q/ [K28.4] character, followed by link configuration parameters over 14 configuration octets (see Table 10), and ends with an /A/ character. Many of the parameters values are of the notation of the value − 1.
- Multiframe 3: Is the same as Multiframe 1.
- Multiframe 4: Is the same as Multiframe 1.

Data Transmission Phase

In the data transmission phase, frame alignment is monitored with control characters. Character replacement is used at the end of frames. Character replacement in the transmitter occurs in the following instances:

- If scrambling is disabled and the last octet of the frame or multiframe equals the octet value of the previous frame.
- If scrambling is enabled and the last octet of the multiframe is equal to 0x7C, or the last octet of a frame is equal to 0xFC.

Table 10. Fourteen Configuration Octets of the ILAS Phase

No.	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	DID[7:0]							
1					BID[3:0]			
2				LID[4:0]				
3	SCR			L[4:0]				
4	F[7:0]							
5				K[4:0]				
6	M[7:0]							
7	CS[1:0]			N[4:0]				
8	SUBCLASS[2:0]			N'[4:0]				
9	JESDV[2:0]			S[4:0]				
10	HD			CF[4:0]				
11	Reserved, Don't Care							
12	Reserved, Don't Care							
13	FCHK[7:0]							

Link Setup Parameters

The following demonstrates how to configure the AD9250 JESD204B interface. The steps to configure the output include the following:

1. Disable lanes before changing configuration
2. Select quick configuration option
3. Configure detailed options
4. Check FCHK, checksum of JESD204B interface parameters
5. Set additional digital output configuration options
6. Re-enable lane(s)

Disable Lanes Before Changing Configuration

Before modifying the JESD204B link parameters, disable the link and hold it in reset. This is accomplished by writing Logic 1 to Register 0x5F, Bit[0].

Select Quick Configuration Option

Write to Register 0x5E, the 204B quick configuration register to select the configuration options. See Table 13 for configuration options and resulting JESD204B parameter values.

- 0x11 = one converter, one lane
- 0x12 = one converter, two lanes
- 0x21 = two converters, one lane
- 0x22 = two converters, two lanes

Configure Detailed Options

Configure the tail bits and control bits.

- With N' = 16 and N = 14, there are two bits available per sample for transmitting additional information over the JESD204B link. The options are tail bits or control bits. By default, tail bits of 0b00 value are used.
- Tail bits are dummy bits sent over the link to complete the two octets and do not convey any information about the input signal. Tail bits can be fixed zeros (default) or psuedo random numbers (Register 0x5F, Bit[6]).
- One or two control bits can be used instead of the tail bits through Register 0x72, Bits[7:6]. The tail bits can be set using Register 0x14, Bits[7:5].

Set lane identification values.

- JESD204B allows parameters to identify the device and lane. These parameters are transmitted during the ILAS phase, and they are accessible in the internal registers.
- There are three identification values: device identification (DID), bank identification (BID), and lane identification (LID). DID and BID are device specific; therefore, they can be used for link identification.

Set number of frames per multiframe, K

- Per the JESD204B specification, a multiframe is defined as a group of K successive frames, where K is between 1 and 32, and it requires that the number of octets be between 17 and 1024. The K value is set to 32 by default in Register 0x70, Bits[7:0]. Note that Register 0x70 represents a value of K − 1.
- The K value can be changed; however, it must comply with a few conditions. The AD9250 uses a fixed value for octets per frame [F] based on the JESD204B quick configuration setting. K must also be a multiple of 4 and conform to the following equation.

$$32 \geq K \geq Ceil\ (17/F)$$

- The JESD204B specification also calls for the number of octets per multiframe (K × F) to be between 17 and 1024. The F value is fixed through the quick configuration setting to ensure this relationship is true.

Table 11. JESD204B Configurable Identification Values

DID Value	Register, Bits	Value Range
LID (Lane 0)	0x66, [4:0]	0…31
LID (Lane 1)	0x67, [4:0]	0…31
DID	0x64, [7:0]	0…255
BID	0x65, [3:0]	0…15

Scramble, SCR.

- Scrambling can be enabled or disabled by setting Register 0x6E, Bit[7]. By default, scrambling is enabled. Per the JESD204B protocol, scrambling is only functional after the lane synchronization has completed.

Select lane synchronization options.

Most of the synchronization features of the JESD204B interface are enabled by default for typical applications. In some cases, these features can be disabled or modified as follows:

- ILAS enabling is controlled in Register 0x5F, Bits[3:2] and by default is enabled. Optionally, to support some unique instances of the interfaces (such as NMCDA-SL), the JESD204B interface can be programmed to either disable the ILAS sequence or continually repeat the ILAS sequence.

The AD9250 has fixed values of some of the JESD204B interface parameters, and they are as follows:

- [N] = 14: number of bits per converter is 14, in Register 0x72, Bits[4:0]; Register 0x72 represents a value of N − 1.
- [N'] = 16: number of bits per sample is 16, in Register 0x73, Bits[4:0]; Register 0x73 represents a value of N' − 1.
- [CF] = 0: number of control words/ frame clock cycle/converter is 0, in Register 0x75, Bits[4:0]

Verify read only values: lanes per link (L), octets per frame (F), number of converters (M), and samples per converter per frame (S). The AD9250 calculates values for some JESD204B parameters based on other settings, particularly the quick configuration register selection. The read only values here are available in the register map for verification.

- [L] = lanes per link can be 1 or 2, read the values from Register 0x6E, Bit[0]
- [F] = octets per frame can be 1, 2, or 4, read the value from Register 0x6F, Bits[7:0]
- [HD] = high density mode can be 0 or 1, read the value from Register 0x75, Bit[7]
- [M] = number of converters per link can be 1 or 2, read the value from Register 0x71, Bits[7:0]
- [S] = samples per converter per frame can be 1 or 2, read the value from Register 0x74, Bits[4:0]

Check FCHK, Checksum of JESD204B Interface Parameters

The JESD204B parameters can be verified through the checksum value [FCHK] of the JESD204B interface parameters. Each lane has a FCHK value associated with it. The FCHK value is transmitted during the ILAS second multiframe and can be read from the internal registers.

The checksum value is the modulo 256 sum of the parameters listed in the No. column of Table 12. The checksum is calculated by adding the parameter fields before they are packed into the octets shown in Table 12.

The FCHK for the lane configuration for data coming out of Lane 0 can be read from Register 0x79. Similarly, the FCHK for the lane configuration for data coming out of Lane 1 can be read from Register 0x7A.

Table 12. JESD204B Configuration Table Used in ILAS and CHKSUM Calculation

No.	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
0	DID[7:0]							
1					BID[3:0]			
2				LID[4:0]				
3	SCR			L[4:0]				
4	F[7:0]							
5				K[4:0]				
6	M[7:0]							
7	CS[1:0]			N[4:0]				
8	SUBCLASS[2:0]			N′[4:0]				
9	JESDV[2:0]			S[4:0]				
10				CF[4:0]				

Additional Digital Output Configuration Options

Other data format controls include the following:

- Invert polarity of serial output data: Register 0x60, Bit[1]
- ADC data format (offset binary or twos complement): Register 0x14, Bits[1:0]
- Options for interpreting single on SYSREF± and SYNCINB±: Register 0x3A
- Option to remap converter and lane assignments, Register 0x82 and Register 0x83. See Figure 50 for simplified block diagram.

Re-Enable Lanes After Configuration

After modifying the JESD204B link parameters, enable the link so that the synchronization process can begin. This is accomplished by writing Logic 0 to Register 0x5F, Bit[0].

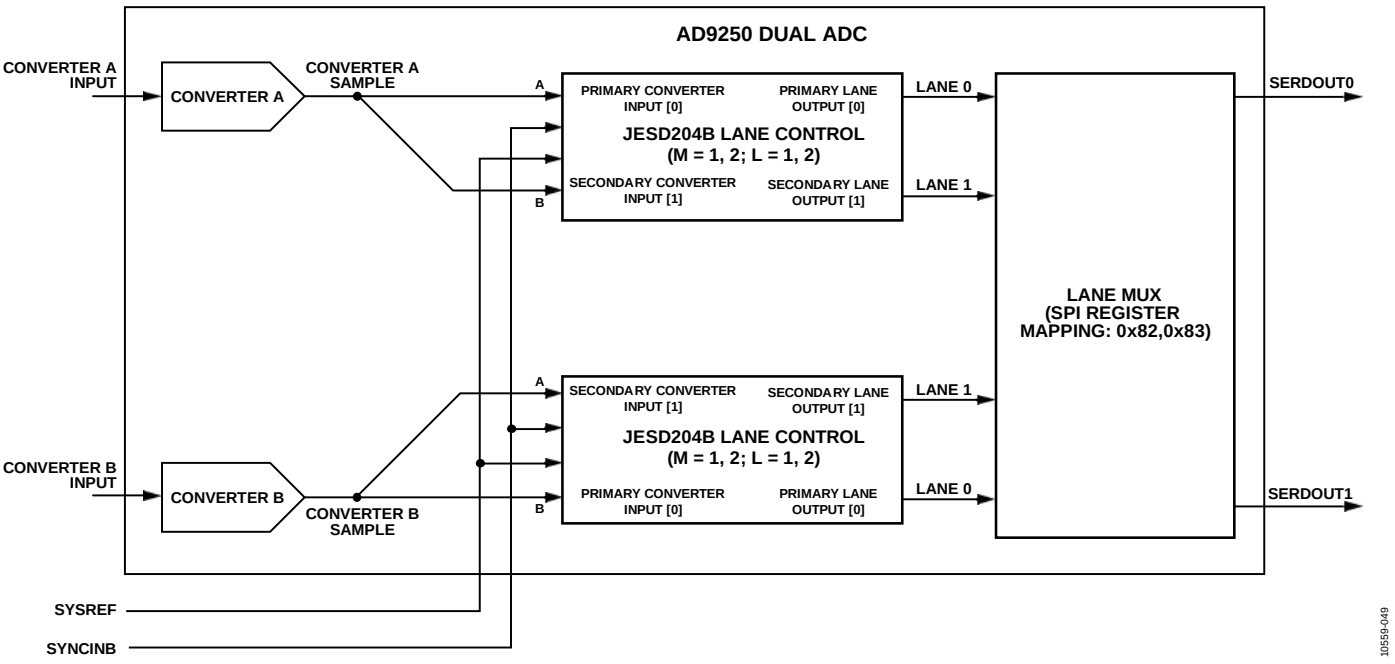

Figure 50. AD9250 Transmit Link Simplified Block Diagram

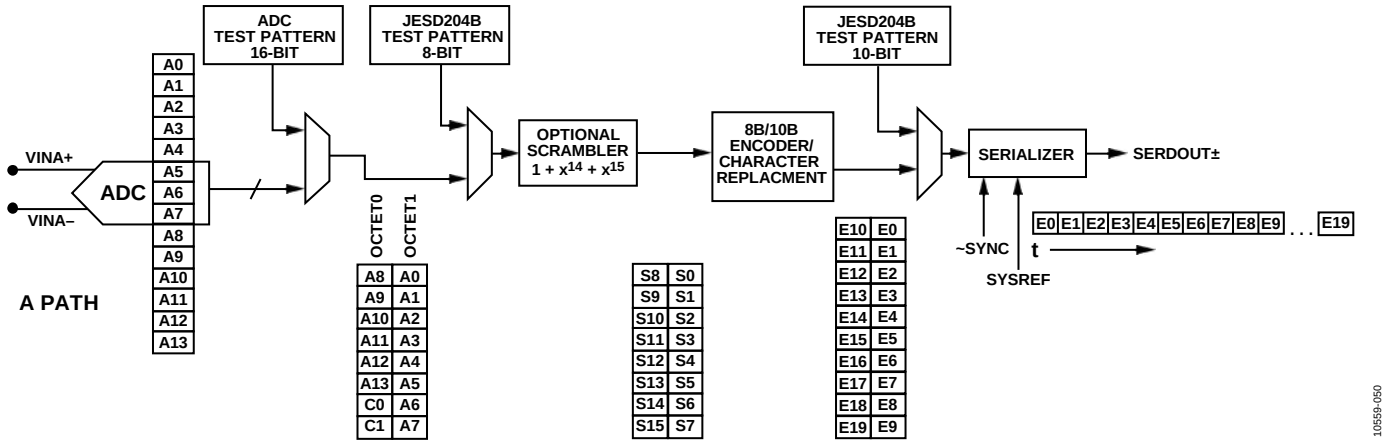

Figure 51. AD9250 Digital Processing of JESD204B Lanes

Table 13. AD9250 JESD204B Typical Configurations

JESD204B Configure Setting	M (No. of Converters), Register 0x71, Bits[7:0]	L (No. of Lanes), Register 0x6E, Bit[0]	F (Octets/Frame), Register 0x6F, Bits[7:0], Read Only	S (Samples/ADC/Frame), Register 0x74, Bits[4:0], Read Only	HD (High Density Mode), Register 0x75, Bit[7], Read Only
0x11	1	1	2	1	0
0x12	1	2	1	1	1
0x21	2	1	4	1	0
0x22 (Default)	2	2	2	1	0

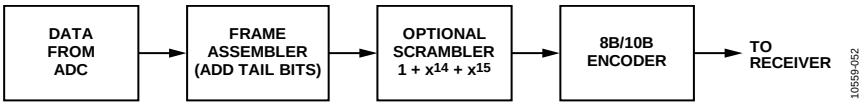

Figure 52. AD9250 ADC Output Data Path

Table 14. AD9250 JESD204B Frame Alignment Monitoring and Correction Replacement Characters

Scrambling	Lane Synchronization	Character to be Replaced	Last Octet in Multiframe	Replacement Character
Off	On	Last octet in frame repeated from previous frame	No	K28.7
Off	On	Last octet in frame repeated from previous frame	Yes	K28.3
Off	Off	Last octet in frame repeated from previous frame	Not applicable	K28.7
On	On	Last octet in frame equals D28.7	No	K28.7
On	On	Last octet in frame equals D28.3	Yes	K28.3
On	Off	Last octet in frame equals D28.7	Not applicable	K28.7

Frame and Lane Alignment Monitoring and Correction

Frame alignment monitoring and correction is part of the JESD204B specification. The 14-bit word requires two octets to transmit all the data. The two octets (MSB and LSB), where F = 2, make up a frame. During normal operating conditions, frame alignment is monitored via alignment characters, which are inserted under certain conditions at the end of a frame. Table 14 summarizes the conditions for character insertion along with the expected characters under the various operation modes. If lane synchronization is enabled, the replacement character value depends on whether the octet is at the end of a frame or at the end of a multiframe.

Based on the operating mode, the receiver can ensure that it is still synchronized to the frame boundary by correctly receiving the replacement characters.

Digital Outputs and Timing

The AD9250 has differential digital outputs that power up by default. The driver current is derived on-chip and sets the output current at each output equal to a nominal 4 mA. Each output presents a 100 Ω dynamic internal termination to reduce unwanted reflections.

Place a 100 Ω differential termination resistor at each receiver input to result in a nominal 300 mV peak-to-peak swing at the receiver (see Figure 53). Alternatively, single-ended 50 Ω termination can be used. When single-ended termination is used, the termination voltage should be DRVDD/2; otherwise, ac coupling capacitors can be used to terminate to any single-ended voltage.

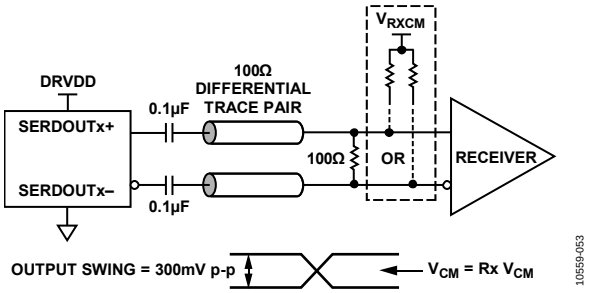

Figure 53. AC-Coupled Digital Output Termination Example

The AD9250 digital outputs can interface with custom ASICs and FPGA receivers, providing superior switching performance in noisy environments. Single point-to-point network topologies are recommended with a single differential 100 Ω termination resistor placed as close to the receiver logic as possible. The common mode of the digital output automatically biases itself to half the supply of the receiver (that is, the common-mode voltage is 0.9 V for a receiver supply of 1.8 V) if dc-coupled connecting is used (see Figure 54). For receiver logic that is not within the bounds of the DRVDD supply, use an ac-coupled connection. Simply place a 0.1 µF capacitor on each output pin and derive a 100 Ω differential termination close to the receiver side.

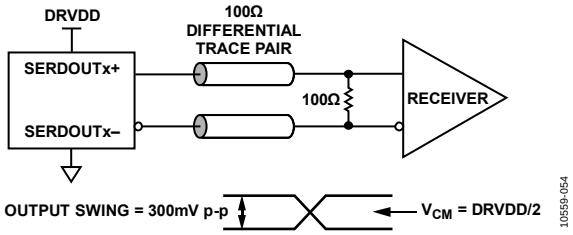

Figure 54. DC-Coupled Digital Output Termination Example

If there is no far-end receiver termination, or if there is poor differential trace routing, timing errors may result. To avoid such timing errors, it is recommended that the trace length be less than six inches, and that the differential output traces be close together and at equal lengths.

Figure 55 shows an example of the digital output (default) data eye and time interval error (TIE) jitter histogram and bathtub curve for the AD9250 lane running at 5 Gbps.

Additional SPI options allow the user to further increase the output driver voltage swing of all four outputs to drive longer trace lengths (see Register 0x15 in Table 17). The power dissipation of the DRVDD supply increases when this option is used. See the Memory Map section for more details.

The format of the output data is twos complement by default. To change the output data format to offset binary, see the Memory Map section (Register 0x14 in Table 17).

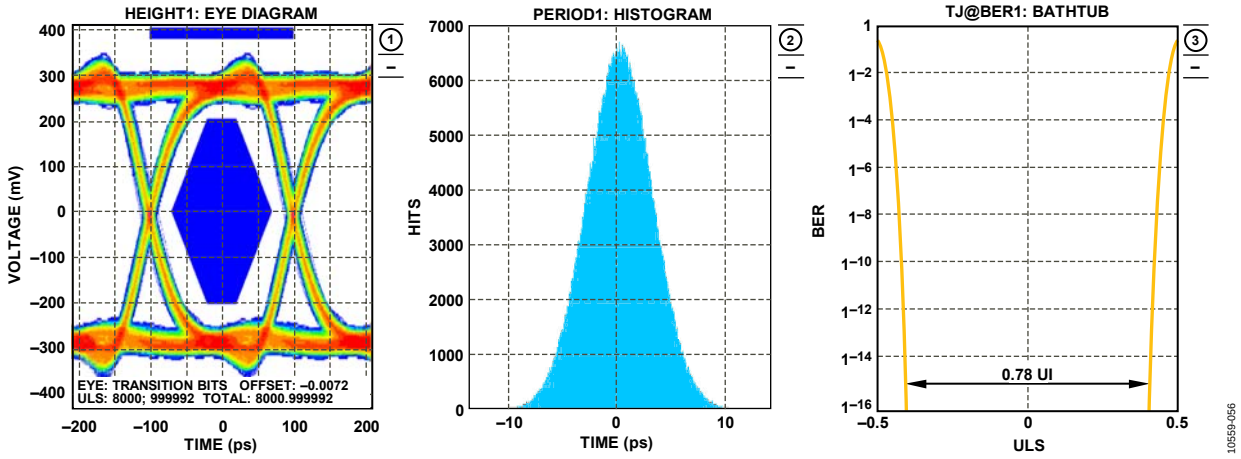

Figure 55. AD9250 Digital Outputs Data Eye, Histogram and Bathtub, External 100 Ω Terminations at 5 Gbps

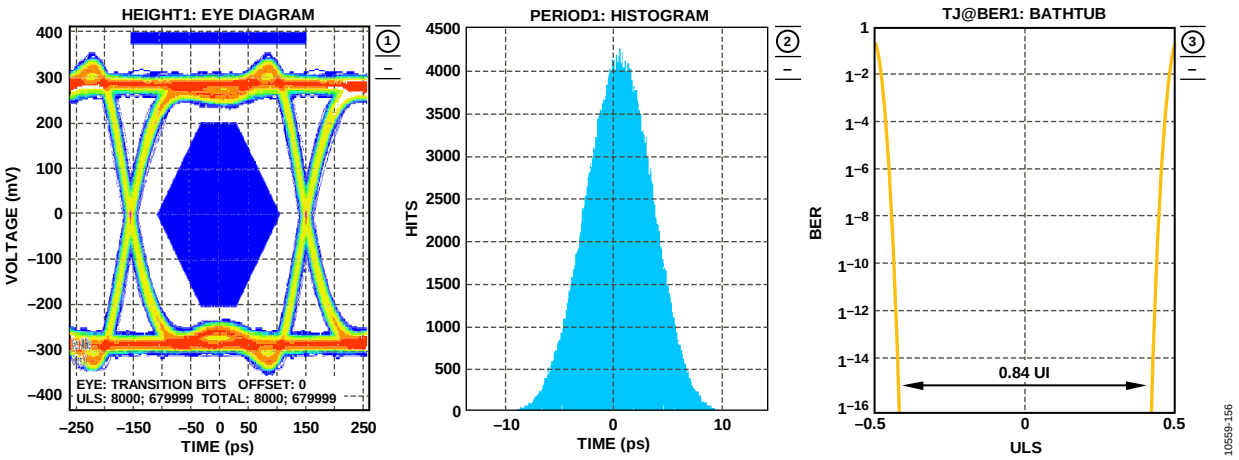

Figure 56. AD9250 Digital Outputs Data Eye, Histogram and Bathtub, External 100 Ω Terminations at 3.4 Gbps

ADC OVERRANGE AND GAIN CONTROL

In receiver applications, it is desirable to have a mechanism to reliably determine when the converter is about to be clipped. The standard overflow indicator provides delayed information on the state of the analog input that is of limited value in preventing clipping. Therefore, it is helpful to have a programmable threshold below full scale that allows time to reduce the gain before the clip occurs. In addition, because input signals can have significant slew rates, latency of this function is of concern.

Using the SPI port, the user can provide a threshold above which the FD output is active. Bit 0 of Register 0x45 enables the fast detect feature. Register 0x47 to Register 0x4A allow the user to set the threshold levels. As long as the signal is below the selected threshold, the FD output remains low. In this mode, the magnitude of the data is considered in the calculation of the condition, but the sign of the data is not considered. The threshold detection responds identically to positive and negative signals outside the desired range (magnitude).

ADC OVERRANGE (OR)

The ADC overrange indicator is asserted when an overrange is detected on the input of the ADC. The overrange condition is determined at the output of the ADC pipeline and, therefore, is subject to a latency of 36 ADC clock cycles. An overrange at the input is indicated by this bit 36 clock cycles after it occurs.

GAIN SWITCHING

The AD9250 includes circuitry that is useful in applications either where large dynamic ranges exist, or where gain ranging amplifiers are employed. This circuitry allows digital thresholds to be set such that an upper threshold and a lower threshold can be programmed.

One such use is to detect when an ADC is about to reach full scale with a particular input condition. The result is to provide an indicator that can be used to quickly insert an attenuator that prevents ADC overdrive.

Fast Threshold Detection (FDA and FDB)

The FD indicator is asserted if the input magnitude exceeds the value programmed in the fast detect upper threshold registers, located in Register 0x47 and Register 0x48. The selected threshold register is compared with the signal magnitude at the output of the ADC. The fast upper threshold detection has a latency of 7 clock cycles. The approximate upper threshold magnitude is defined by

Upper Threshold Magnitude (dBFS) = 20 log (*Threshold Magnitude*/2^{13})

Or, alternatively, the register value can be calculated by the target threshold using the following equation:

$$Value = 10^{(Threshold\ Magnitude\ [dBFS]/20)} \times 2^{13}$$

The FD indicators are not cleared until the signal drops below the lower threshold for the programmed dwell time. The lower threshold is programmed in the fast detect lower threshold registers, located at Register 0x49 and Register 0x4A. The fast detect lower threshold register is a 13-bit register that is compared with the signal magnitude at the output of the ADC. This comparison is subject to the ADC pipeline latency but is accurate in terms of converter resolution. The lower threshold magnitude is defined by

Lower Threshold Magnitude (dBFS) = 20 log (*Threshold Magnitude*/2^{13})

For example, to set an upper threshold of −6 dBFS, write 0x0FFF to those registers; and to set a lower threshold of −10 dBFS, write 0x0A1D to those registers.

The dwell time can be programmed from 1 to 65,535 sample clock cycles by placing the desired value in the fast detect dwell time registers, located in Register 0x4B and Register 0x4C.

The operation of the upper threshold and lower threshold registers, along with the dwell time registers, is shown in Figure 57.

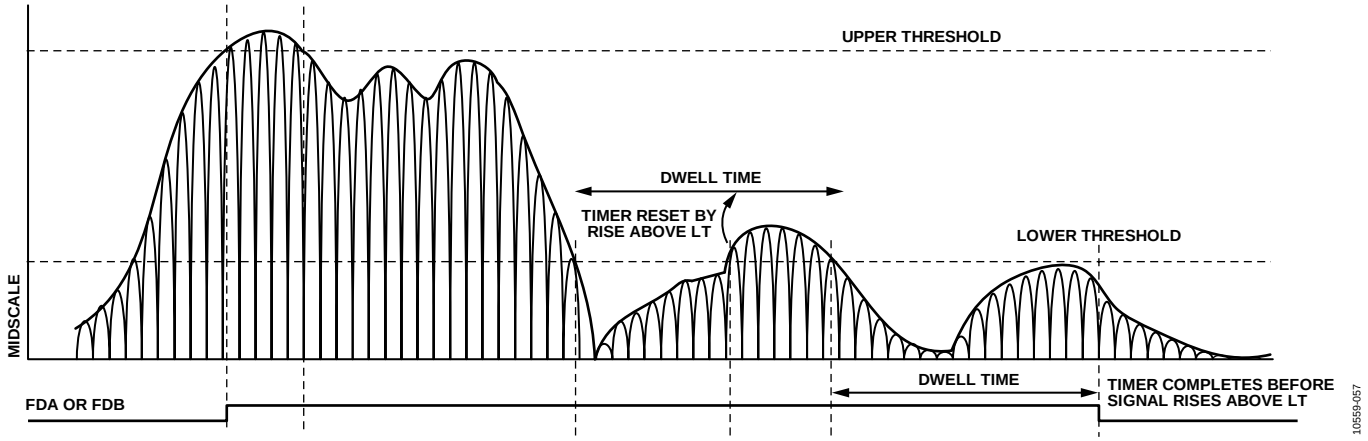

Figure 57. Threshold Settings for FDA and FDB Signals

DC CORRECTION

Because the dc offset of the ADC may be significantly larger than the signal being measured, a dc correction circuit is included to null the dc offset before measuring the power. The dc correction circuit can also be switched into the main signal path; however, this may not be appropriate if the ADC is digitizing a time-varying signal with significant dc content, such as GSM.

DC CORRECTION BANDWIDTH

The dc correction circuit is a high-pass filter with a programmable bandwidth (ranging between 0.29 Hz and 2.387 kHz at 245.76 MSPS). The bandwidth is controlled by writing to the 4-bit dc correction bandwidth select register, located at Register 0x40, Bits[5:2]. The following equation can be used to compute the bandwidth value for the dc correction circuit:

$$DC\_Corr\_BW = 2^{-k-14} \times f_{CLK}/(2 \times \pi)$$

where:
k is the 4-bit value programmed in Bits[5:2] of Register 0x40 (values between 0 and 13 are valid for k).
f_{CLK} is the AD9250 ADC sample rate in hertz.

DC CORRECTION READBACK

The current dc correction value can be read back in Register 0x41 and Register 0x42 for each channel. The dc correction value is a 16-bit value that can span the entire input range of the ADC.

DC CORRECTION FREEZE

Setting Bit 6 of Register 0x40 freezes the dc correction at its current state and continues to use the last updated value as the dc correction value. Clearing this bit restarts dc correction and adds the currently calculated value to the data.

DC CORRECTION (DCC) ENABLE BITS

Setting Bit 1 of Register 0x40 enables dc correction for use in the output data signal path.

SERIAL PORT INTERFACE (SPI)

The AD9250 SPI allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. The SPI gives the user added flexibility and customization, depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields. These fields are documented in the Memory Map section. For detailed operational information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

CONFIGURATION USING THE SPI

Three pins define the SPI of this ADC: the SCLK pin, the SDIO pin, and the $\overline{CS}$ pin (see Table 15). The SCLK (serial clock) pin is used to synchronize the read and write data presented from/to the ADC. The SDIO (serial data input/output) pin is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The $\overline{CS}$ (chip select bar) pin is an active low control that enables or disables the read and write cycles.

Table 15. Serial Port Interface Pins

Pin	Function
SCLK	Serial Clock. The serial shift clock input, which is used to synchronize serial interface, reads and writes.
SDIO	Serial Data Input/Output. A dual-purpose pin that typically serves as an input or an output, depending on the instruction being sent and the relative position in the timing frame.
$\overline{CS}$	Chip Select Bar. An active low control that gates the read and write cycles.

The falling edge of $\overline{CS}$, in conjunction with the rising edge of SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 58 and Table 5.

Other modes involving the $\overline{CS}$ are available. The $\overline{CS}$ can be held low indefinitely, which permanently enables the device; this is called streaming. The $\overline{CS}$ can stall high between bytes to allow for additional external timing. When $\overline{CS}$ is tied high, SPI functions are placed in a high impedance mode. This mode turns on any SPI pin secondary functions.

During an instruction phase, a 16-bit instruction is transmitted. Data follows the instruction phase, and its length is determined by the W0 and the W1 bits.

All data is composed of 8-bit words. The first bit of each individual byte of serial data indicates whether a read or write command is issued. This allows the SDIO pin to change direction from an input to an output.

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to be used both to program the chip and to read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the SDIO pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or in LSB first mode. MSB first is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

HARDWARE INTERFACE

The pins described in Table 15 comprise the physical interface between the user programming device and the serial port of the AD9250. The SCLK pin and the $\overline{CS}$ pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

Do not activate the SPI port during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the $\overline{CS}$ signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9250 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

SPI ACCESSIBLE FEATURES

Table 16 provides a brief description of the general features that are accessible via the SPI. These features are described in detail in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. The AD9250 part-specific features are described in the Memory Map Register Description section.

Table 16. Features Accessible Using the SPI

Feature Name	Description
Mode	Allows the user to set either power-down mode or standby mode
Clock	Allows the user to access the DCS via the SPI
Offset	Allows the user to digitally adjust the converter offset
Test I/O	Allows the user to set test modes to have known data on output bits
Output Mode	Allows the user to set up outputs
Output Phase	Allows the user to set the output clock polarity
Output Delay	Allows the user to vary the DCO delay
VREF	Allows the user to set the reference voltage

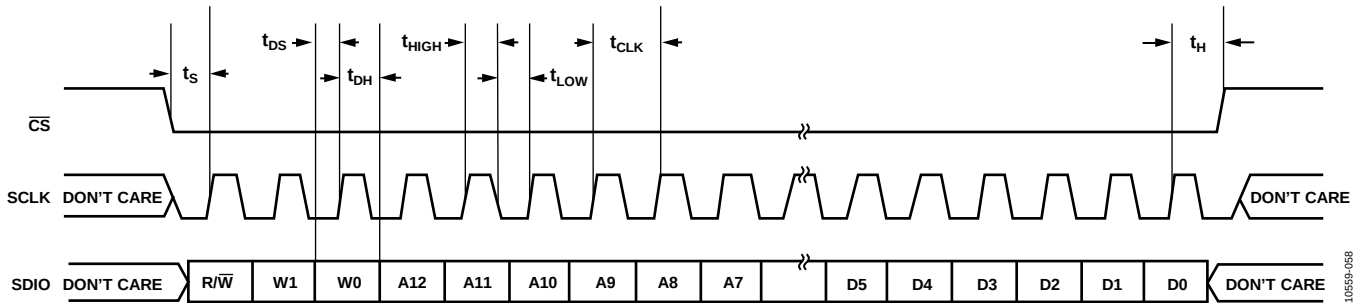

Figure 58. Serial Port Interface Timing Diagram

MEMORY MAP

READING THE MEMORY MAP REGISTER TABLE

Each row in the memory map register table has eight bit locations. The memory map is roughly divided into three sections: the chip configuration registers (Address 0x00 to Address 0x02); the channel index and transfer registers (Address 0x05 and Address 0xFF); and the ADC functions registers, including setup, control, and test (Address 0x08 to Address 0xA8).

The memory map register table (see Table 17) documents the default hexadecimal value for each hexadecimal address shown. The column with the heading Bit 7 (MSB) is the start of the default hexadecimal value given. For example, Address 0x14, the output mode register, has a hexadecimal default value of 0x01. This means that Bit 0 = 1, and the remaining bits are 0s. This setting is the default output format value, which is twos complement. For more information on this function and others, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. This document details the functions controlled by Register 0x00 to Register 0x25. The remaining registers, Register 0x3A and Register 0x59, are documented in the Memory Map Register Description section.

Open and Reserved Locations

All address and bit locations that are not included in Table 17 are not currently supported for this device. Unused bits of a valid address location should be written with 0s. Writing to these locations is required only when part of an address location is open (for example, Address 0x18). If the entire address location is open (for example, Address 0x13), do not write to this address location.

Default Values

After the AD9250 is reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table, Table 17.

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "bit is set to Logic 1" or "writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "bit is set to Logic 0" or "writing Logic 0 for the bit."

Transfer Register Map

Address 0x09, Address 0x0B to Address 0x14, Address 18, Address 3A, Address 0x40 to Address 0x4C are shadowed. Writes to these addresses do not affect part operation until a transfer command is issued by writing 0x01 to Address 0xFF, setting the transfer bit. This allows these registers to be updated internally and simultaneously when the transfer bit is set. The internal update takes place when the transfer bit is set, and then the bit autoclears.

Channel-Specific Registers

Some channel setup functions, such as the signal monitor thresholds, can be programmed to a different value for each channel. In these cases, channel address locations are internally duplicated for each channel. These registers and bits are designated in Table 17 as local. These local registers and bits can be accessed by setting the appropriate Channel A or Channel B bits in Register 0x05. If both bits are set, the subsequent write affects the registers of both channels. In a read cycle, only Channel A or Channel B should be set to read one of the two registers. If both bits are set during an SPI read cycle, the part returns the value for Channel A. Registers and bits designated as global in Table 17 affect the entire part and the channel features for which independent settings are not allowed between channels. The settings in Register 0x05 do not affect the global registers and bits.

MEMORY MAP REGISTER TABLE

All address and bit locations that are not included in Table 17 are not currently supported for this device.

Table 17. Memory Map Registers

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x00	Global SPI config	0	LSB first	Soft reset	1	1	Soft reset	LSB first	0	0x18	
0x01	CHIP ID	AD9250 8-bit CHIP ID is 0xB9								0xB9	Read only
0x02	Chip info			Speed grade 00 = 250 MSPS 11 = 170 MSPS			Reserved for chip die revision currently 0x0			0x00 or 0x30	
0x05	Channel index							SPI write to ADC B path	SPI write to ADC A path	0x03	
0x08	PDWN modes			External PDWN mode; 0 = PDWN is full power down; 1 = PDWN puts device in standby	JTX in standby; 0 = 204B core is unaffected in standby; 1: 204B core is powered down except for PLL during standby	JESD204B power modes; 00 = normal mode (power up); 01 = power-down mode: PLL off, serializer off, clocks stopped, digital held in reset; 10 = standby mode: PLL on, serializer off, clocks stopped, digital held in reset		Chip power modes; 00 = normal mode (power up); 01 = power-down mode, digital datapath clocks disabled, digital datapath held in reset; most analog paths powered off; 10 = standby mode; digital datapath clocks disabled, digital datapath held in reset, some analog paths powered off		0x00	
0x09	Global clock	Reserved		Clock selection: 00 = Nyquist clock 10 = RF clock divide by 4 11 = clock off					Clock duty cycle stabilizer enable	0x01	DCS enabled if clock divider enabled
0x0A	PLL status	PLL locked status							204B link is ready		Read only
0x0B	Global clock divider			Clock divider phase output of the internal divide by 1 to divide by 8 divider circuit, clock cycles are relative to the input clock to this block; 0x0 = 0 input clock cycles delayed; 0x1 = 1 input clock cycles delayed; 0x2 = 2 input clock cycles delayed; ….. 0x7 = 7 input clock cycles delayed Note that the RF clock divider phase is not selectable			Clock divider ratio of the divide by 1 to divide by 8 divider circuit to generate the encode clock; 0x00 = divide by 1; 0x01 = divide by 2; 0x02 = divide by 3; ….. 0x7 = divide by 8; using a CLKDIV_DIVIDE_RATIO > 0 (Divide Ratio > 1) causes the DCS to be automatically enabled		0x00	
0x0D	Test control reg	User test mode cycle; 00 = repeat pattern (user pattern 1, 2, 3, 4, 1, 2, 3, 4, 1, …); 10 = single pattern (user pattern 1, 2, 3, 4, then all zeros)		Long psuedo random number generator reset; 0 = long PRN enabled; 1 = long PRN held in reset	Short psuedo random number generator reset; 0 = short PRN enabled; 1 = short PRN held in reset	Data output test generation mode; 0000 = off (normal mode); 0001 = midscale short; 0010 = positive Full scale; 0011 = negative full scale; 0100 = alternating checker board; 0101 = PN sequence long; 0110 = PN sequence short; 0111 = 1/0 word toggle; 1000 = user test mode (use with Register 0x0D, Bit[7] and user pattern 1, 2, 3, 4); 1001 to 1110 = unused; 1111 = ramp output				0x00	
0x0E	BIST test						Reset BIST		BIST enable	0x00	

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x10	Customer offset	Offset adjust in LSBs from +31 to −32 (twos complement format); 01 1111 = adjust output by +31; 01 1110 = adjust output by +30; … 00 0001 = adjust output by +1; 00 0000 = adjust output by 0 [default]; … 10 0001 = adjust output by −31; 10 0000 = adjust output by −32								0x00	
0x14	Output mode	JTX CS bits assignment (in conjunction with Register 0x72) 000 = {overrange||underrange, valid} 001 = {overrange||underrange} 010 = {overrange||underrange, blank} 011 = {blank, valid} 100 = {blank, blank} All others = {overrange||underrange, valid}			Disable output from ADC		Invert ADC data; 0 = normal (default); 1 = inverted	Digital datapath output data format select (DFS) (local); 00 = offset binary; 01 = twos complement		0x01	
0x15	CML output adjust						JESD204B CML differential output drive level adjustment; 000 = 81% of nominal (that is, 238 mV); 001 = 89% of nominal (that is, 262 mV); 010 = 98% of nominal (that is, 286 mV); 011 = nominal [default] (that is, 293 mV); 110 = 126% of nominal (that is, 368 mV)			0x03	
0x18	ADC VREF				Main reference full-scale VREF adjustment; 0 1111 = internal 2.087 V p-p; ... 0 0001 = internal 1.772 V p-p; 0 0000 = internal 1.75 V p-p [default]; 1 1111 = internal 1.727 V p-p; … 1 0000 = internal 1.383 V p-p					0x00	
0x19	User Test Pattern 1 L	User Test Pattern 1 LSB; use in conjunction with Register 0x0D and Register 0x61								0x00	
0x1A	User Test Pattern 1 M	User Test Pattern 1 MSB								0x00	
0x1B	User Test Pattern 2 L	User Test Pattern 2 LSB								0x00	
0x1C	User Test Pattern 2 M	User Test Pattern 2 MSB								0x00	
0x1D	User Test Pattern 3 L	User Test Pattern 3 LSB								0x00	
0x1E	User Test Pattern 3 M	User Test Pattern 3 MSB								0x00	
0x1F	User Test Pattern 4 L	User Test Pattern 4 LSB								0x00	
0x20	User Test Pattern 4 M	User Test Pattern 4 MSB								0x00	
0x21	PLL low encode				00 = for lane speeds > 2 Gbps; 01 = for lane speeds < 2 Gbps					0x00	
0x3A	SYNCINB±/ SYSREF± CTRL				0 = normal mode; 1 = realign lanes on every active SYNCINB±	0 = normal mode; 1 = realign lanes on every active SYSREF±	SYSREF± mode; 0 = continuous reset clock dividers; 1 = sync on next SYSREF± rising edge only	SYSREF± enable; 0 = disabled; 1 = enabled	Enable SYSREF± buffer; 0 = buffer enabled; 1 = buffer disabled	0x00	

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x40	DCC CTRL		Freeze dc correction; 0 = calculate; 1 = freezeval	DC correction bandwidth select; correction bandwidth is 2387.32 Hz/reg val; there are 14 possible values; 0000 = 2387.32 Hz; 0001 = 1193.66 Hz; 1101 = 0.29 Hz				Enable DCC		0x00	
0x41	DCC value LSB	DC Correction Value[7:0]								0x00	
0x42	DCC value MSB	DC Correction Value[15:8]								0x00	
0x45	Fast detect control				Pin function; 0 = fast detect; 1 = overrange	Force FDA/FDB pins; 0 = normal function; 1 = force to value	Force value of FDA/FDB pins if force pins is true, this value is output on FD pins		Enable fast detect output	0x00	
0x47	FD upper threshold	Fast Detect Upper Threshold[7:0]								0x00	
0x48	FD upper threshold		Fast Detect Upper Threshold[12:8]							0x00	
0x49	FD lower threshold	Fast Detect Lower Threshold[7:0]								0x00	
0x4A	FD lower threshold		Fast Detect Lower Threshold[12:8]							0x00	
0x4B	FD dwell time	Fast Detect Dwell Time[7:0]								0x00	
0x4C	FD dwell time	Fast Detect Dwell Time[15:8]								0x00	
0x5E	204B quick config	Quick configuration register, always reads back 0x00; 0x11 = M = 1, L = 1; one converter, one lane; second converter is not automatically powered down; 0x12 = M = 1, L = 2; one converter, two lanes; second converter is not automatically powered down; 0x21 = M = 2, L = 1; two converters, one lane; 0x22 = M = 2, L = 2; two converters, two lanes								0x00	Always reads back 0x00
0x5F	204B Link CTRL 1		Tail bits: If CS bits are not enabled; 0 = extra bits are 0; 1 = extra bits are 9-bit PN	JESD204B test sample enabled	Reserved; set to 1	ILAS mode; 01 = ILAS normal mode enabled; 11 = ILAS always on, test mode		Reserved; set to 0	Power-down JESD204B link; set high while configuring link parameters	0x14	
0x60	204B Link CTRL 2	Reserved; set to 0	Reserved; set to 0	Reserved; set to 0				Invert logic of JESD204B bits		0x00	
0x61	204B Link CTRL 3	Reserved; set to 0	Reserved; set to 0	Test data injection point; 01 = 10-bit data at 8b/10b output; 10 = 8-bit data at scrambler input		JESD204B test mode patterns; 0000 = normal operation (test mode disabled); 0001 = alternating checker board; 0010 = 1/0 word toggle; 0011 = PN sequence PN23; 0100 = PN sequence PN9; 0101= continuous/repeat user test mode; 0110 = single user test mode; 0111 = reserved; 1000 = modified RPAT test sequence, must be used with JTX_TEST_GEN_SEL = 01 (output of 8b/10b); 1100 = PN sequence PN7; 1101 = PN sequence PN15; other setting are unused			0x00	
0x62	204B Link CTRL 4	Reserved								0x00	

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0x63	204B Link CTRL 5	Reserved								0x00	
0x64	204B DID config	JESD204B DID value								0x00	
0x65	204B BID config					JESD204B BID value				0x00	
0x66	204B LID Config 1				Lane 0 LID value					0x00	
0x67	204B LID Config 2				Lane 1 LID value					0x01	
0x6E	204B parameters SCR/L	JESD204B scrambling (SCR); 0 = disabled; 1 = enabled							JESD204B lanes (L); 0 = 1 lane; 1 = 2 lanes	0x81	
0x6F	204B parameters F	JESD204B number of octets per frame (F); calculated value (Note that this value is in x – 1 format]								0x01	Read Only
0x70	204B parameters K	JESD204B number of frames per multiframe (K); set value of K per JESD204B specifications, but also must be a multiple of 4 octets (Note that this value is in x – 1 format]								0x1F	
0x71	204B parameters M	JESD204B number of converters (M); 0 = 1 converter; 1 = 2 converters								0x01	
0x72	204B parameters CS/N	Number of control bits (CS); 00 = no control bits (CS = 0); 01 = 1 control bit (CS = 1); 10 = 2 control bits (CS = 2)				ADC converter resolution (N), 0xD = 14-bit converter (N = 14) (Note that this value is in x – 1 format]				0x0D	
0x73	204B parameters subclass/Np		JESD204B subclass; 0x0 = Subclass 0; 0x1 = Subclass 1 (default)			JESD204B N′ value; 0xF = N′ = 16 (Note that this value is in x – 1 format]				0x2F	
0x74	204B parameters S			Reserved; set to 1	JESD204B samples per converter frame cycle (S); read only (Note that this value is in x – 1 format)					0x20	
0x75	204B parameters HD and CF	JESD204B HD value; read only			JESD204B control words per frame clock cycle per link (CF); read only					0x00	Read Only
0x76	204B RESV1	Reserved Field Number 1								0x00	
0x77	204B RESV2	Reserved Field Number 2								0x00	
0x79	204B CHKSUM0	JESD204B serial checksumvalue for Lane 0								0x42	
0x7A	204B CHKSUM1	JESD204B serial checksumvalue for Lane 1								0x43	
0x82	204B Lane Assign 1			00 = assign Logical Lane 0 to Physical Lane A [default]; 01 = assign Logical Lane 0 to Physical Lane B				Reserved; set to 1	Reserved; set to 0	0x02	
0x83	204B Lane Assign 2			Reserved; set to 1	Reserved; set to 1			00 = assign Logical Lane 1 to Physical Lane A; 01 = assign Logical Lane 1 to Physical Lane B [default]		0x31	
0x8B	204B LMFC offset				Local multiframe clock (LMFC) phase offset value; reset value for LMFC phase counter when SYSREF is asserted; used for deterministic delay applications					0x00	

Reg Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default	Notes
0xA8	204B pre-emphasis	JESD204B pre-emphasis enable option (consult factory for more detail); set value to 0x04 for pre-emphasis off; set value to 0x14 for pre-emphasis on								0x04	Typically not required
0xFF	Device update (global)								Transfer settings		

MEMORY MAP REGISTER DESCRIPTION

For more information on functions controlled in Register 0x00 to Register 0x25, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

APPLICATIONS INFORMATION

DESIGN GUIDELINES

Before starting system level design and layout of the AD9250, it is recommended that the designer become familiar with these guidelines, which discuss the special circuit connections and layout requirements needed for certain pins.

Power and Ground Recommendations

When connecting power to the AD9250, it is recommended that two separate 1.8 V power supplies be used: the power supply for AVDD can be isolated and for DVDD and DRVDD it can be tied together, in which case an isolation inductor of approximately 1 µH is recommended. Alternately, the JESD204B PHY power (DRVDD) and analog (AVDD) supplies can be tied together, and a separate supply can be used for the digital outputs (DVDD).

The designer can employ several different decoupling capacitors to cover both high and low frequencies. Locate these capacitors close to the point of entry at the PC board level and close to the pins of the part with minimal trace length.

When using the AD9250, a single PCB ground plane should be sufficient. With proper decoupling and smart partitioning of the PCB analog, digital, and clock sections, optimum performance is easily achieved.

Exposed Paddle Thermal Heat Slug Recommendations

It is mandatory that the exposed paddle on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance. Mate a continuous, exposed (no solder mask) copper plane on the PCB to the AD9250 exposed paddle, Pin 0.

The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be filled or plugged with nonconductive epoxy.

To maximize the coverage and adhesion between the ADC and the PCB, overlay a silkscreen to partition the continuous plane on the PCB into several uniform sections. This provides several tie points between the ADC and the PCB during the reflow process. Using one continuous plane with no partitions guarantees only one tie point between the ADC and the PCB. See the evaluation board for a PCB layout example. For detailed information about the packaging and PCB layout of chip scale packages, refer to the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

VCM

Decouple the VCM pin to ground with a 0.1 µF capacitor, as shown in Figure 36. For optimal channel-to-channel isolation, include a 33 Ω resistor between the AD9250 VCM pin and the Channel A analog input network connection, as well as between the AD9250 VCM pin and the Channel B analog input network connection.

SPI Port

When the full dynamic performance of the converter is required, do not activate the SPI port during periods. Because the SCLK, $\overline{\text{CS}}$, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9250 to keep these signals from transitioning at the converter input pins during critical sampling periods.

OUTLINE DIMENSIONS

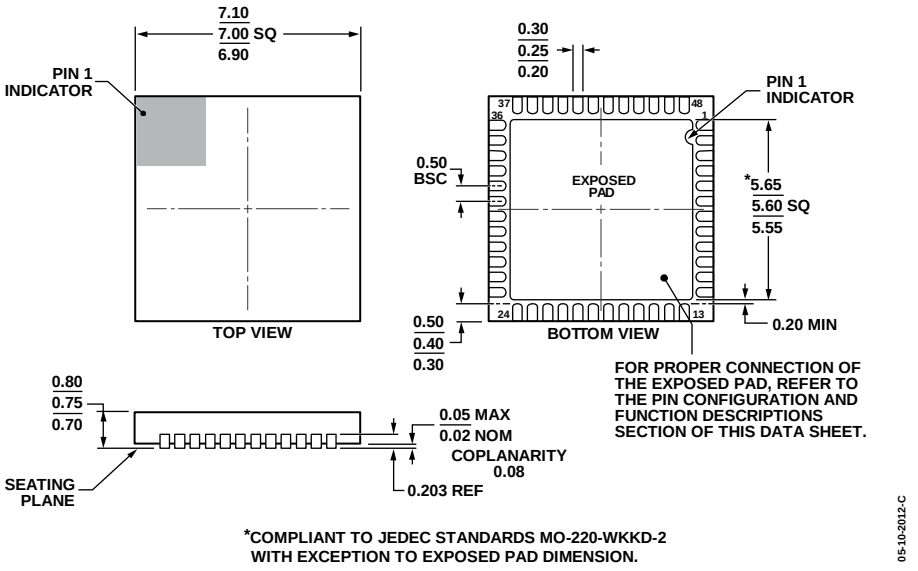

Figure 59. 48-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
7 mm × 7 mm Body, Very Very Thin Quad
(CP-48-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9250BCPZ-170	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-48-13
AD9250BCPZRL7-170	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-48-13
AD9250-170EBZ	−40°C to +85°C	Evaluation Board with AD9250-170	
AD9250BCPZ-250	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-48-13
AD9250BCPZRL7-250	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-48-13
AD9250-250EBZ	−40°C to +85°C	Evaluation Board with AD9250-250	

[1] Z = RoHS Compliant Part.

Page 42 of 44, Page 43 of 44, and Page 44 of 44 are blank.

More JESD204 Information

Useful Links

www.jedec.org

www.analog.com/JESD204

www.xilinx.com/products/intellectual-property/EF-DI-JESD204.htm

www.planetanalog.com/author.asp?section_id=3041&doc_id=561117&

www.electronicdesign.com/analog/pair-right-jesd204b-converter-your-fpga

www.eetimes.com/document.asp?doc_id=1280943

www.electronicdesign.com/analog/kickstart-your-system-designs-jesd204b

Videos

Rapid Prototyping with JESD204B Using FMC and Xilinx FPGAs

A Look at the JESD204B Serial Interface EYE Diagram

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